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QUANTUM-DOT CELLULAR AUTOMATA-BASED SUPERIOR DESIGN OF CONSERVATIVE REVERSIBLE PARITY LOGIC CIRCUITS

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ABSTRACT

Quantum-dot Cellular Automata (QCA) is an innovative technology in the nano-scale for changing the CMOS revolution with an alternative one. It provides some benefits in reversible logic, like competitive power consumption and feature size. Therefore, much attention is paid to producing different reversible circuits using that technique. This paper presents a superior model for a reversible Feynman gate-based odd parity generator and checker. The proposed model can be utilized for loss bit detection /checking in telecommunication systems. The circuit verification is carried out using the QCADesigner tool. The proposed Feynman gate provides an improvement of 50% and 48% in terms of latency and cost, respectively. The parity generator, parity checker and nano-communication circuit have complexity reduction by 25%, 37% and 24%, respectively, in terms of requiring cells.

KEYWORDS

QCA, Reversible gate, Parity generator, Parity checker.

1. INTRODUCTION

In 1965, a table for integrated CMOS devices inside a chip was predicted by Moore [1]. The devices in this table grow exponentially as Moore described. Over time, the number of devices within the chip will reach the maximum value, so that it cannot be increased due to physical restrictions. This motivated scientists to think about new solutions to replace CMOS in order to keep Moore's table continuing. The QCA paradigm is one of the new nanotechnologies explored in 1993 by Lent et al. [2] as a CMOS alternative in digital systems [3]. This technology has a different computational paradigm compared to CMOS [4]. The basic building block in this nano-technique is a quantum cell. QCA cell has a square shape injected with two electrons [5]. The Coulomb repulsion of electrons enforces it to localize at corners. Because there are only two probabilities for localizing the electrons, QCA cells can represent binary numbers. Reversible circuits for parity generator and parity checker are necessary in telecommunication systems for the self-detection of errors [6]. This paper presents a new QCA structure of the reversible Feynman gate. The presented gate is used for designing a new form of reversible parity generator/checker. The QCADesigner tool [7] will be used in default parameters to display the input/output waveforms.

This paper will be organized as follows:

Section 2 will give a QCA background, while Section 3 will explain the reversible Feynman gate. Sections 4 will show the reversible Odd-Parity Generator/Checker and Section 5 will explain the proposed nano-communication system module. Section 6 will detail the simulation results and comparison and finally, the conclusion will be presented in Section 7.

2. BACKGROUND

This section provides an overview of QCA technology in terms of the main unit and working principle.

2.1 QCA Basics

The QCA-based design consists of a group of cells. Each cell contains four holes (dots) and two particles (electrons) [8]-[9]. These particles have the ability to tunnel between dots inside the cell, but cannot

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escape out [10]. The Coulomb interaction forces the electrons to settle in a diagonal position depending on the driver cell [11]. Cell polarization is illustrated in Figure 1, where P=1 represents (logic1) and P=-1 represents (logic 0) [12]. QCA wire and many logic functions can be constructed by arranging a set of cells.

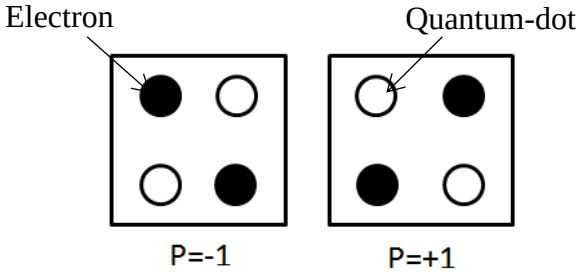


Figure 1. QCA cell polarization [13].

2.2 QCA Wire

The QCA wire consists of a group of primary cells, where it transfers the logical value from input to output and the Coulomb interaction transfers the polarization from one cell to another [14]-[15]. The two main configurations of QCA wire are illustrated in Figure 2.

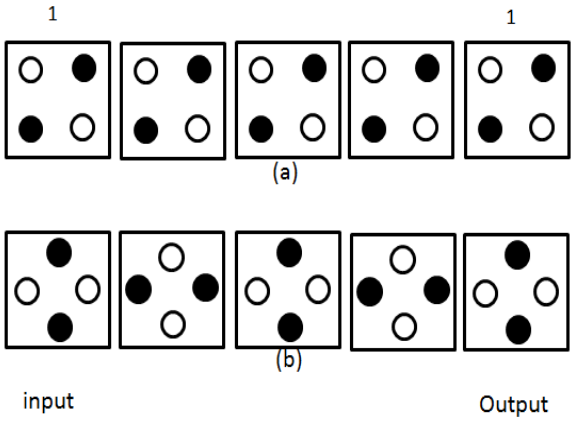


Figure 2. QCA binary wire (a) Normal arrangement (b) Rotated arrangement [15].

2.3 QCA Building Units

The dominant block in QCA circuits is the majority gate, where when applying any input to 1 or 0, the AND or OR gate can be obtained [16]-[17]. Many researchers paid attention to this gate as in [18]-[20]. The majority gate with three inputs is presented in two forms, as shown in Figure 3 [21]. The general formula of this gate is given by:

$$\mathrm{Maj}_{(A,B,C)} = AB + BC + CA \tag{1}$$

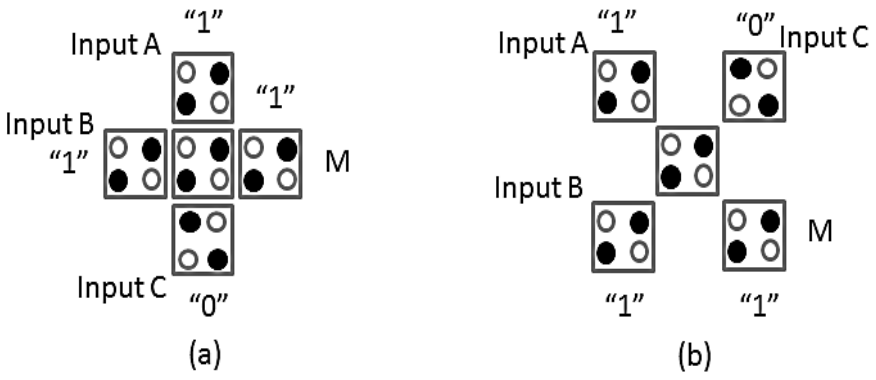


Figure 3. Majority gate layouts.

The primary building blocks in QCA are inverter and majority gate, where it is possible to design any logic circuit with these blocks only [22]. The three configurations of the QCA inverter are shown in Figure 4.

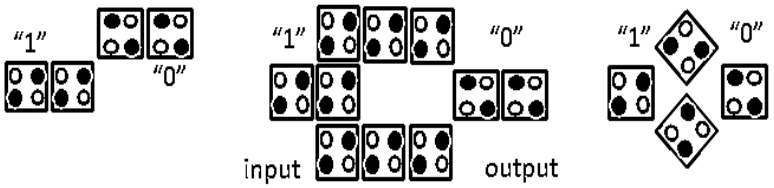


Figure 4. QCA inverter layouts.

2.4 QCA Clock Signal

The computation and synchronization in QCA are done using the clock signal [23]. Clocking is important also for letting the information flow from input to output [11], [24]. The barrier level is essential for tunnelling the electrons between dots, where it can be controlled by the clock signal. The polarization of cell remains unclear as long as the clocking is low. Whenever the clocking reaches the highest level, the cell gets its fixed polarization. Adiabatic switching is essential in QCA by splitting the clock signal into four phases (switch, hold, release and relax), where the QCA circuit can be divided further into four clock zones. Figure 5 illustrated this process [25]-[26].

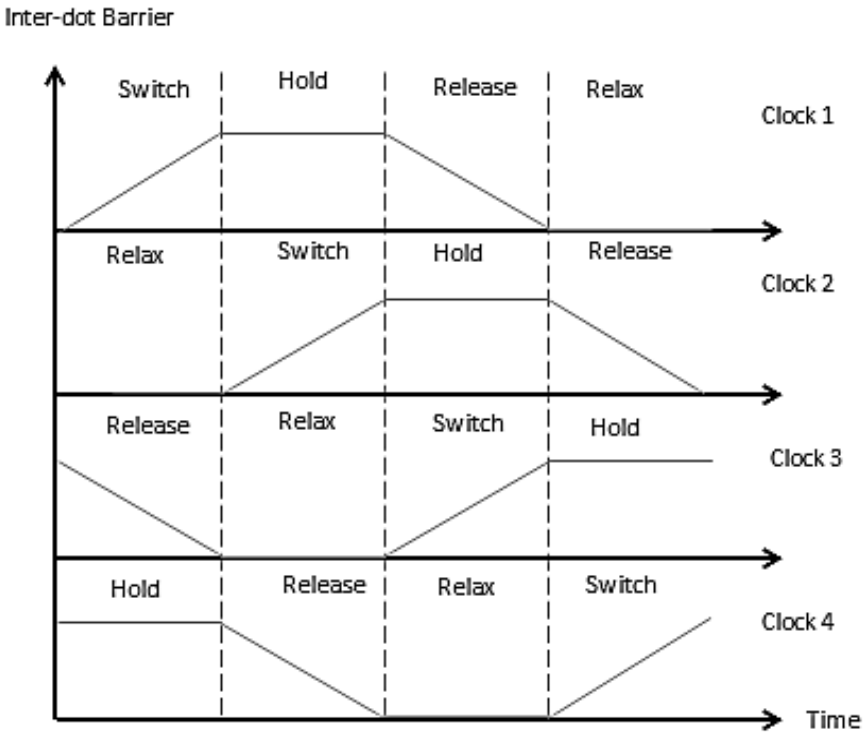


Figure 5. Clock signal phases in four zones.

3. REVERSIBLE FEYNMAN GATE

The Feynman gate is a logic reversible block that receives 2 inputs (X1 and X2) and generates 2 outputs (M and N). The input value can be identified by the output value because, there is a one-to-one matching between the input-output values. Output equations can be expressed as follows:

M=x1 and N=X1⊕X2. The Feynman logic diagram [6] and the proposed QCA layout with input/output waveforms are shown in Figure 6. The proposed Feynman gate, inspired from the XOR gate given by [27], has many advantages, such as its complexity=11 cells and area=0.00096 μm^2 with latency=0.25

clock cycle. These features make its superior compared with previous designs. A QCA cell generally has two electrons. These particles change their position depending on the principle of electron repulsion and are affected by the driver cell as well as the surrounding cells. Therefore, several QCA gates have been suggested in the literature taking advantage of this potential, such as [28]-[29]. The QCA-XOR gate used in this work was derived from QCA's inherent capability and did not follow any Boolean function. The performance of the proposed gate in terms of power consumption is achieved using the estimator tool called QCAPro [30]. The average energy dissipated (leakage and switching) can be calculated in three different levels of King Energy (0.5 E_k, 1 E_k and 1.5 E_k) using this tool, as detailed in Figure 7. The output as observed from the simulation waveforms can be expressed as in Table 1.

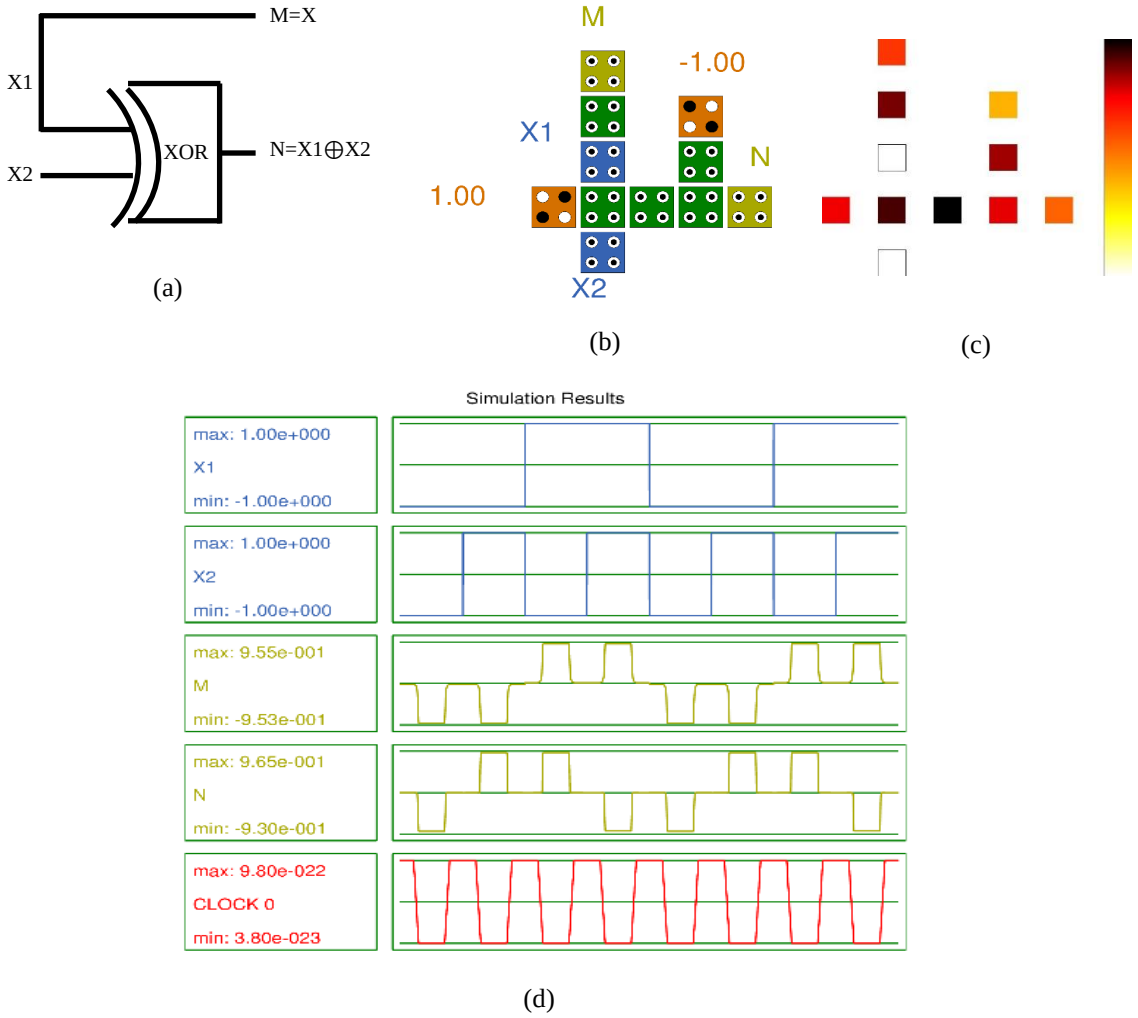


Figure 6. Feynman gate (a) Logic diagram [6], (b) QCA form (c) Power map at 0.5 E_k and (d) Simulation waveforms.

Table 1. Input-output Feynman gate.

X1	X2	M	N
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

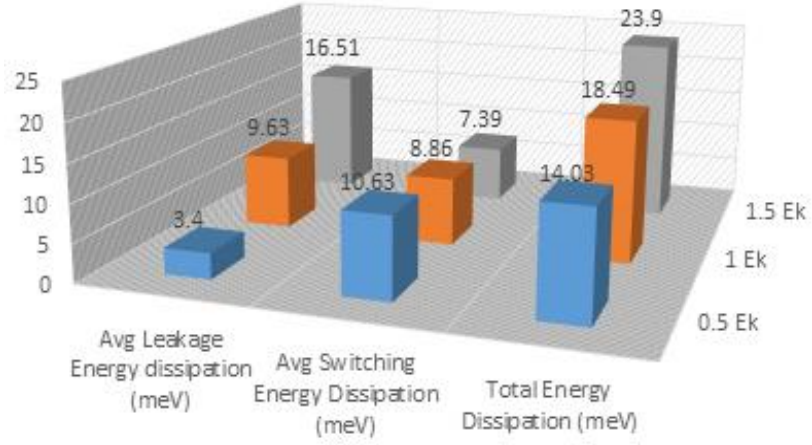


Figure 7. Power consumption of the proposed gate in three different levels.

4. REVERSIBLE ODD-PARITY GENERATOR / CHECKER

The odd-parity generator has been designed utilizing a cascade of proposed Feynman gates. The parity-bit generator gives an output when applying three values (X1, X2 and X3) at the inputs. The logic diagrams with QCA form are illustrated in Figure 8. The wonderful feature of the proposed generator reduces the complexity by 0.25%, where it has complexity=24 cells and area=0.035 μm^2 with latency=0.75 clock cycle.

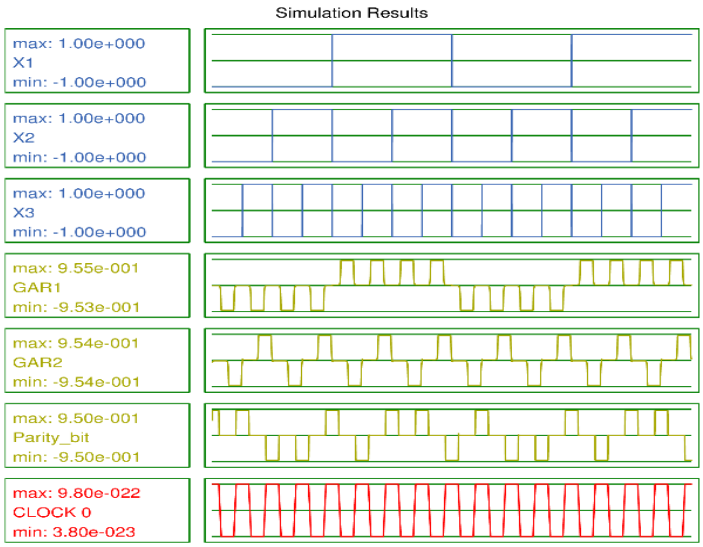


Figure 8. Reversible odd parity generator (a) Logic diagram [6] (b) Proposed QCA form and (c) Simulation results.

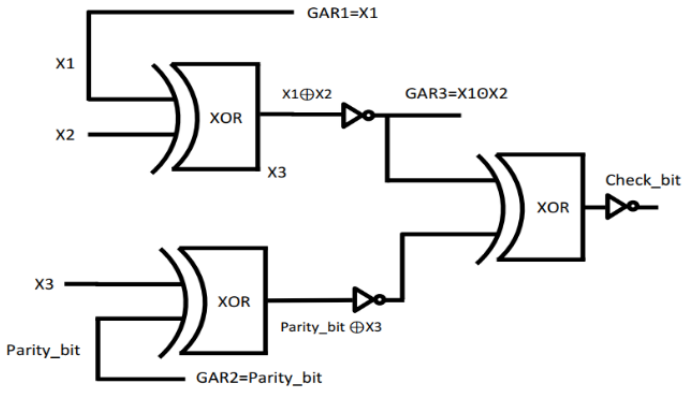
The extra parity-bit forms a message word with an odd number of 1's, where if the four-bit message received contains even 1's, that indicates an error to have occurred in the transmission. The input-output odd parity as observed from the simulation results shown in Figure 8c can be expressed as illustrated in Table 2.

The parity checker is utilized for checking whether an error that occurs at the parity-bit has been previously added in the message at the transmitter. Check-bit=1 when the number of 1's becomes even at the message word (input message includes parity-bit) indicating an occurring error; otherwise, check-bit=0 when error-free. The reversible odd-parity checker produces an output by applying XNOR operation for the input bits and parity-bit. Figure 9 illustrates the logic diagram and proposed QCA layout with simulation results.

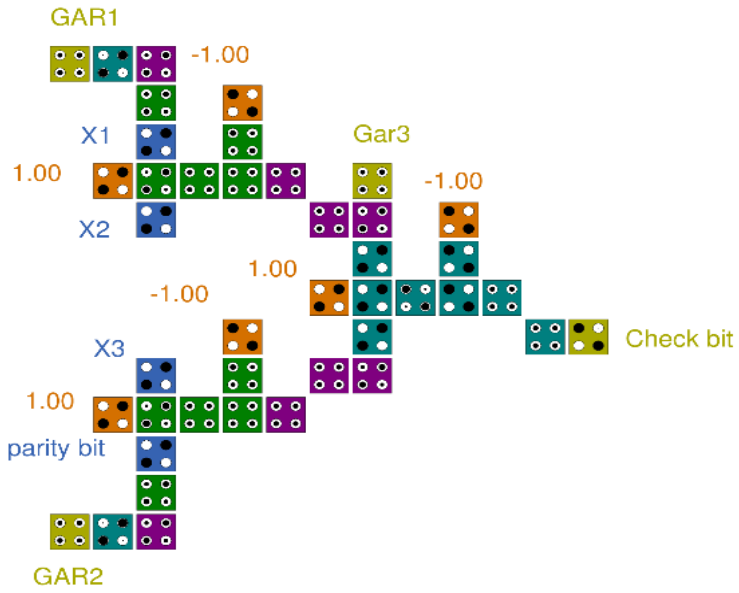
Table 2. Input-output odd parity generator.

X1	X2	X3	GAR1	GAR2	Parity-bit
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	1	0

The wonderful feature of the proposed odd parity checker is that using a coherence vector simulation engine reduces the complexity by 0.37%, where it has complexity=42 cells and area=0.06 μm^2 with latency=0.75 clock cycle. Table 3 explains the input-output binary data as observed from the simulation results shown in Figure 9c.



(a)



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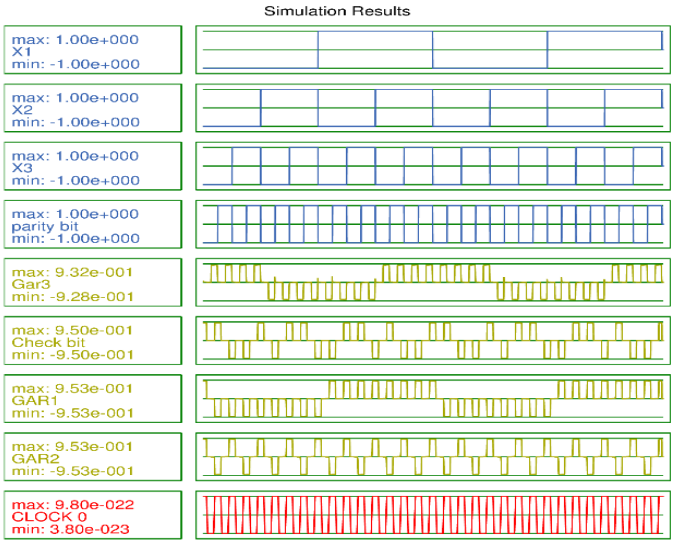

(c)

Figure 9. Reversible odd parity checker (a) Logic diagram [6] (b) Proposed QCA layout (c) Simulation results.

Table 3. Input-output odd parity checker.

X1	X2	X3	Parity bit	GAR1	GAR2	GAR3	Check bit
0	0	0	0	0	0	1	1
0	0	0	1	0	1	1	0
0	0	1	0	0	0	1	0
0	0	1	1	0	1	1	1
0	1	0	0	0	0	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	0	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	1	0	1	0
1	1	1	1	1	1	1	1

5. THE PROPOSED NANO-COMMUNICATION SYSTEM MODULE

For the nano-communication system, the self-checking is important for error detection in telecommunication networks. An optimal nano-communication system has been performed utilizing the proposed reversible generator/checker (odd-parity). The proposed module has been constructed by three separated blocks (transmitter, receiver and transmission medium). The transmitter generates an extra bit (parity bit) as a tail of three input message bits to form a pattern with an odd number of 1's.

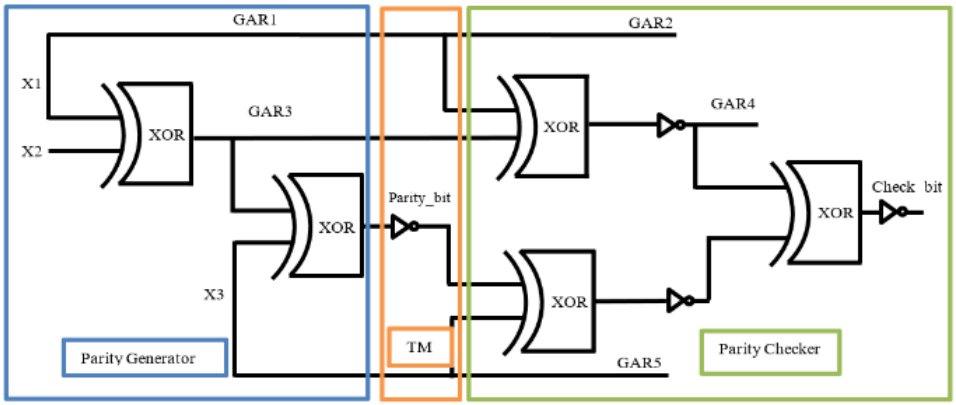

Figure 10. Nano-communication system block diagram proposed by [6].

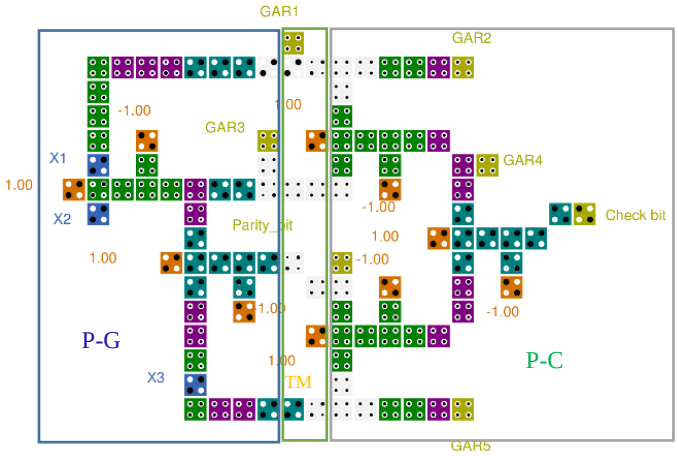

Figure 11. Proposed QCA layout of the nano-communication system.

The receiver receives the message word that contains the tail (parity bit) which has been generated by the transmitter. The receiver checks the parity bit for detecting whether an error has occurred. The message pattern is error-free if it contains an odd number of 1's; otherwise, the receiver indicates an occurring error through the transmission. Figure 10 illustrates the module logic diagram, while the proposed QCA form of the nano-communication system is shown in Figure 11. The proposed module requires 106 cells only and the occupation area=0.14 μm^2 with delay latency=1.75 clock cycle. The transmission medium is a link between transmitter and receiver. The message word includes the parity bit sent to the receiver *via* a transmission medium. The truth table of the nano-communication system is illustrated in Table 4.

Table 4. Nano-communication system truth table.

Parity Generator by transmitter				Parity Checker				
message word			Parity bit	Received Message by receiver				Check bit
0	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	0	0
0	1	1	1	0	1	1	1	0
1	0	0	0	1	0	0	0	0
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	0	1	0
1	1	1	0	1	1	1	0	0

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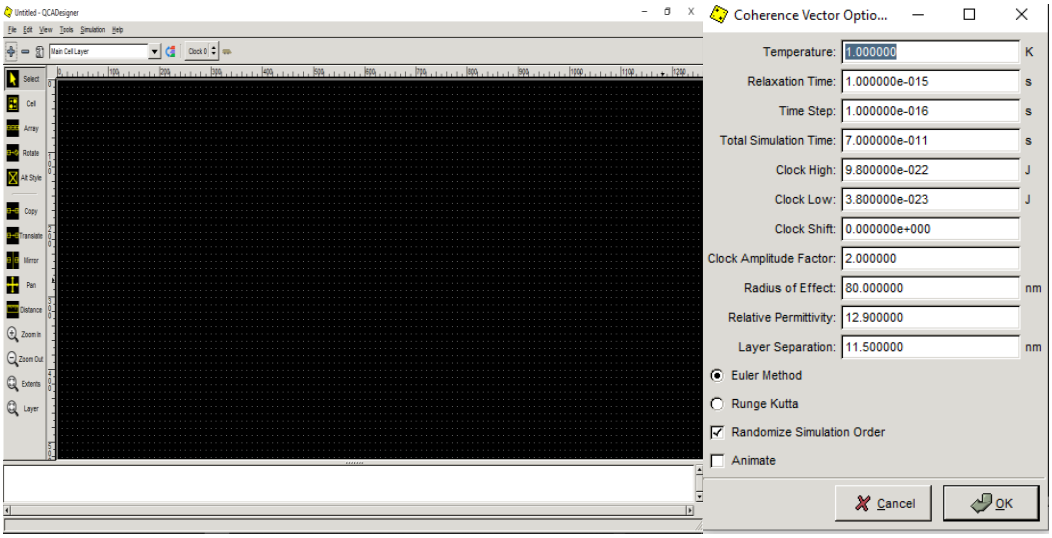
6. SIMULATION RESULTS AND PERFORMANCE COMPARISON

The QCADesigner simulation tool V2.0.3 with default parameters has been used for verifying the performance of the proposed circuits. This tool is more flexible in handling cells and circuit design. Further, circuit simulation is carried out with the same tool to show the output waveforms. In this work, this tool is used in default parameters and the screen layout with parameters is shown in Figure 12. The simulation results are illustrated in Figures 6d, 8c, 9c and 13. The proposed QCA layouts are superior in many aspects, such as area, number of cells needed and minimum delay latency. A comparison between existing and proposed designs is illustrated in Table 5. In QCA technology, many factors have been presented to compare circuits, such as delay, complexity, area and cost. The cost function in the QCA has been presented in several approaches. In this research, the cost function is calculated as the approach presented in [31]. The proposed Feynman gate provides an improvement of 50% and 48% in terms of latency and cost, respectively. The parity generator gives an improvement of 25 % and 20% in terms of cell count and cost, while the improvements for the proposed parity checker are as follows: 26%, 37%, 25% and 65% in terms of area, cell count, latency and cost, respectively. In addition, the proposed nano-communication system gives improvements of 10%, 24%, 13% and 40% in terms of area, cell count, latency and cost, respectively.



(a) (b)

Figure 12. QCADesigner tool (a) Screen layout, (b) Default parameters.

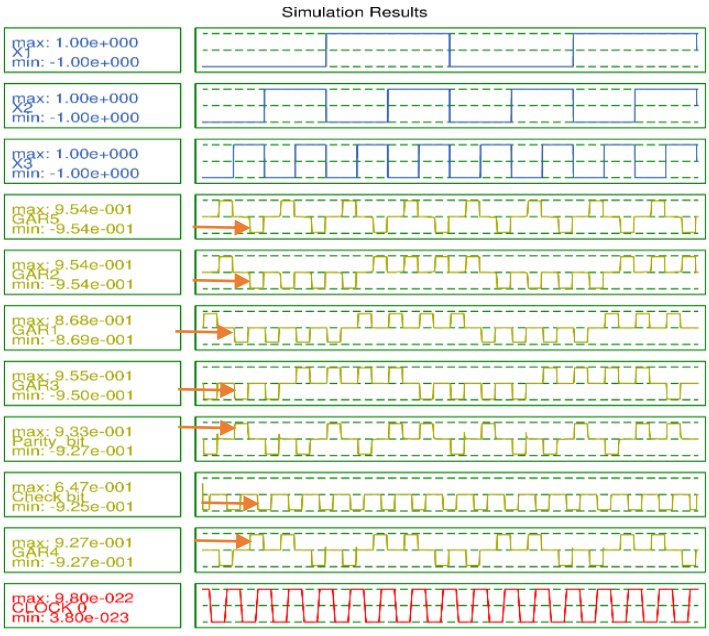


Figure 13. The input/output waveforms of the proposed nano-communication system.

Table 5. Comparison of the proposed circuits with existing designs.

QCA Circuit	Area (μm^2)	Cell Count	Latency	Cost (Area*Delay*Complexity)
Feynman Gate [32]	0.112	90	1.75	17.64
Feynman Gate [33]	0.038	43	0.75	1.2255
Feynman Gate [34]	0.08	75	1.25	7.5
Feynman Gate [35]	0.038	54	0.5	1.026
Feynman Gate [36]	0.07	53	0.75	2.7825
Feynman Gate [37]	0.038	34	0.75	0.969
Feynman Gate [6]	0.017	16	0.5	0.136
Feynman Gate [38]	0.0092	11	0.5	0.0506
proposed Feynman Gate	0.0096	11	0.25	0.0264
Parity Generator [33]	0.078	72	1.75	9.828
Parity Generator [6]	0.033	32	0.75	0.792
Proposed Parity Generator	0.035	24	0.75	0.63
Parity Checker [33]	0.143	130	2	37.18
Parity Checker [6]	0.081	67	1	5.427
Proposed Parity Checker	0.06	42	0.75	1.89
Nano-Communication Circuit [33]	0.479	293	2	280.694
Nano-Communication Circuit [6]	0.155	140	2	43.4
Proposed Nano-Communication Circuit	0.14	106	1.75	25.97

7. CONCLUSION

Designing a logic circuit in the nano-level is the goal of scientists in the digital world. QCA technology is one of many proposed solutions. This paper introduces a new QCA layout of odd parity bit circuit (generator and checker). The presented design is in optimal form and implemented based on the proposed layout of the QCA Feynman gate. An efficient nano-communication system is accomplished using the proposed generator and checker circuit. This system has the ability to self-check the error that might occur in message words during transmission. The proposed QCA layout has a superior performance in many metrics used in QCA circuit, such as area, delay (latency) and complexity (cell count) in comparison with conventional presented circuits. The proposed circuits have been verified using QCADesigner tool V 2.0.3 with default parameters.

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ملخص البحث:

تُعد آليات النُّقط الكمية الخلوية ذاتية التشغيل تقنيةً مبتكرة في نطاق تكنولوجيا النانو من أجل الاستعاضة عن ثورة تقنية (CMOS) بأخرى بديلة. وهي توفر بعض الفوائد في المنطق القابل للقلب؛ مثل الاستهلاك المنافس للقدرة، وحجم السِّمات. من هنا، اتجه الكثير من الاهتمام الى إنتاج داراتٍ قابلةٍ للقلْب باستخدام تلك التقنية المبتكرة.

تقدم هذه الورقة البحثية أنموذجاً متفوقاً لمولدٍ وفاحصٍ للتكافؤ الفردي استناداً على بوابة "فاينمان" قابلةٍ للقلْب. ومن الممكن الاستفادة من الأنموذج المقترح في الكشف عن أو فحص الفقْد في أنظمة الاتصال. وقد تم التحقق من دارات الأنموذج باستخدام أداة (QCADesigner). وتوفر بوابة "فاينمان" المقترحة تحسيناً بنسبة (50%) و (48%) من حيث التأخير، والكلفة على الترتيب. وقد قللت: مولد التكافؤ، وفاحص التكافؤ، ودارة اتصالات النانو درجة التعقيد من حيث عدد الخلايا المطلوبة بنسبة (25%) و (37%) و (24%) على الترتيب.