

# C-ELEMENT DESIGN IN QUANTUM DOT CELLULAR AUTOMATA

Mutaz Al-Tarawneh and Ziyad A. Altarawneh

(Received: 30-Aug.-2020, Revised: 14-Oct.-2020, Accepted: 5-Nov.-2020)

## ABSTRACT

The continuous market demands for high-performance and energy-efficient computing systems have steered the computational paradigm and technologies towards nano-scale quantum dot cellular automata (QCA). This paper presents novel simple and complex QCA-based C-element structures. The proposed structures were thoroughly analyzed based on key design parameters, such as area, energy dissipation and robustness against structural defects. Simulation results demonstrate that the proposed simple structures have achieved up to 56% and 66% improvement in area and energy dissipation, respectively. On the other hand, the complex structures have shown a profound immunity against structural defects and achieved up to 143% improvement as compared to the simple structures. The proposed C-element structures can be considered as viable blocks for asynchronous designs.

## KEYWORDS

QCA, Asynchronous circuits, C-Element, Robustness, Structural defects.

## 1. INTRODUCTION

Over the past few decades, the microelectronics industry has been driven by increasing market demands for enhanced integration, energy efficiency and speed of integrated circuits (ICs). This was done primarily by scaling the transistor feature size and by implementing specific device architectures, such as FinFET and Gate-All-Around (GAA) nanowires [1]-[3]. Nonetheless, as the transistor feature size is reduced, some issues, like power consumption and increased leakage current, are beginning to dominate device performance due to various quantum effects and increased process variation levels at nano-scale, halting the advantages of device scaling being adopted. According to the International Technology Roadmap for Semiconductors (ITRS), the development of new computational paradigms and device structures is inevitable in future technology nodes with regard to device technology and clocking strategies [2], [4]. In this context, the nano-scale Quantum-dot Cellular Automata (QCA) technology is one potential alternative that is anticipated to overrule the VLSI technology and deliver rapid advancements in the internet of things (IoT) era [5] and information security [6]. The concept of QCA was first introduced in [7]. Unlike conventional CMOS-based structures, in which information is transferred by the flow of electrical current, QCA depends on the coulombic interaction between adjacent cells. In addition, the polarization level of the confined electrons within a QCA cell represents the binary levels in QCA-based structures. This ultimately allows the QCA-based structure to surpass CMOS-based counterparts in terms of switching speed, device density and power consumption [8]-[9]. Hence, QCA is considered as a transistor-less technology which can serve as a replacement technology to design nano-scale digital circuits [10]-[12].

Typically, QCA devices are described on the basis of symmetric square cells, whereby all computational logic gates and memory structures can be correctly imitated. These structures can be implemented by assembling QCA cells in a specific geometric pattern to achieve the desired logic function. In QCA technology, the primitive building blocks are the majority voter and inverter gates, as shown in Figure 1. The conventional AND and OR logic gates can be simply implemented based on the 3-input majority gate by setting one of the inputs to either "0" or "1", respectively. An important issue in the design of QCA circuits is the switching of QCA cells from one state to another that is controlled by external clock signals. A clock signal has four sequential phases; namely, switch, hold, release and relax [13], as depicted in Figure 2.

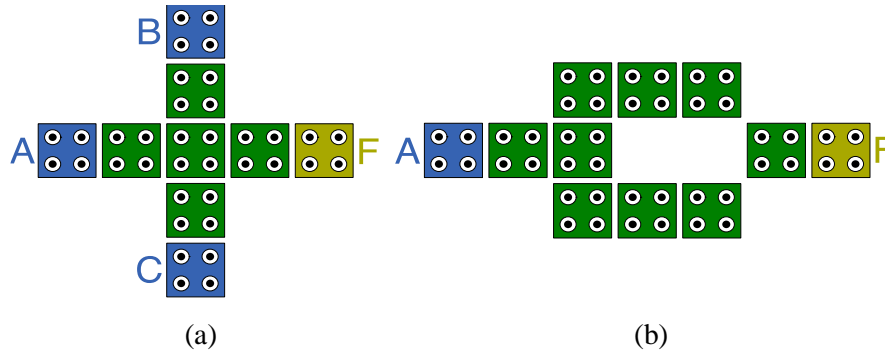


Figure 1. Basic QCA building blocks: (a) Majority gate, (b) Inverter.

The purpose of these phases is to allow or deny the tunneling of the confined electrons in a QCA cell and in turn, achieving stable logic states and information flow by controlling the inter-dot barrier of a cell [14]. In addition, the QCA cells in a particular structure are typically grouped into sequential sub-arrays known as clock zones. The clock signals applied to consecutive clock zones are phase-shifted by 90 degrees to synchronize the polarization change within the QCA structure and prevent back-propagation of information between adjacent cells assigned to different clocking zones, as shown in Figure 3.

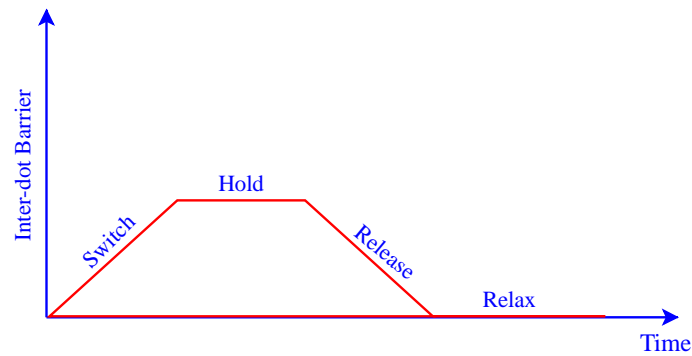


Figure 2. QCA clock phases.

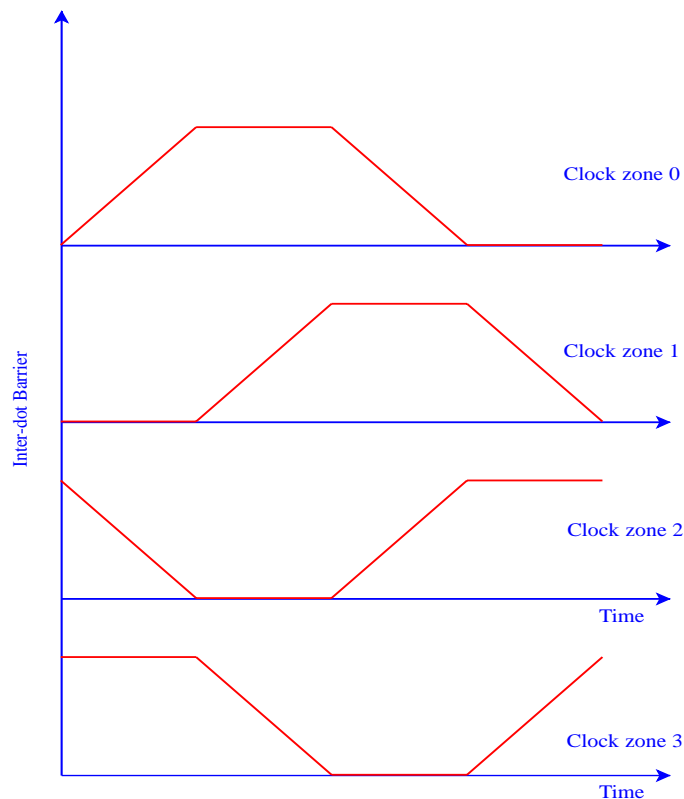


Figure 3. QCA clock zones.

Recently, extensive research efforts have been made on the design of various computational logic and memory structures, such as adders [15]-[18], multiplexers [19]-[20] and memory elements [21]-[23] based on QCA technology. More recently, Bahar et al. [11] have introduced effective single-layer binary discrete cosine transform (BinDCT) using QCA technology. In addition, the authors of [24] have proposed a QCA-based architecture of a new single-layer butterfly switching network (BSN) as a multistage interconnection network (MIN) for parallel computing. Moreover, the authors of [25] have implemented a bit-serial adder (BSA) using modified majority gate and E-shaped exclusive-OR gate. Additionally, Marshal et al. [26] have proposed novel and cost-efficient QCA-based configurable logic blocks and memory blocks, that can be used in Field Programmable Gate Array (FPGA) and embedded systems' designs. Furthermore, Song et al. [12] have suggested a novel loop-based RAM cell with asynchronous set and reset, based on a new 2-1 multiplexer and D-latch structures. Apparently, the variety of QCA-based logic and memory structures introduces QCA technology as a substantial candidate for a new computing paradigm.

A key factor in designing QCA-based structures is the reliability against structural defects. These defects can be categorized as dislocation defects that are caused by cells moving around their axis, dopant defects in which a QCA cell may have one or more extra or missing dots, interstitial (i.e., cell displacement) defects where cells may deviate from their intended horizontal or vertical orientation and vacancy defects (i.e., cell missing) caused by complete absence of cells. The presence of such defects in a computational structure may be manifested as an error that compromises the expected functionality of a design [27].

In recent years, asynchronous circuit designs have received considerable significance in the VLSI scientific community [28]-[30]. Such designs pose a great potential for low-power and high-performance computing and network-on-chip systems [31]. Asynchronous circuit designs can be used to ensure correct communication between different frequency domains. One of the most frequently used structures in constructing asynchronous circuits is the C-element, known as Muller gate [32]. This peculiar structure serves as a primitive building block in several asynchronous logic designs and is used in implementing the synchronization required by most handshaking schemes, which provides the basis for asynchronous communication, especially in micro-pipelines and some network-on-chip designs [31]-[34]. Figure 4 represents the symbolic representation of the 2-input C-element and Table 1 demonstrates its truth table. Its output (F) only changes when the inputs (A and B) have equal logical values. However, when the inputs (A and B) are different, the output (F) memorizes its previous logical state.

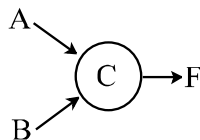


Figure 4. Symbolic representation of 2-input C-element.

Table 1. 2-Input C-element truth table.

A	B	$F_i$
0	0	0
0	1	$F_{i-1}$
1	0	$F_{i-1}$
1	1	1

The purpose of this paper is to propose various QCA implementations of the C-element. As far as the authors could verify, there is no previous research efforts to tackle QCA-based C-element designs. This paper presents different QCA-based C-element structures with thorough analysis of their area, energy dissipation and robustness against structural defects. The proposed designs include 2-, 3- and 4-input C-elements.

The rest of this paper is organized as follows. Section 2 shows the proposed C-element structures. Section 3 presents the simulation results and compares the proposed structures in terms of their area, energy dissipation and robustness. Finally, Section 4 summarizes and concludes the paper.

## 2. PROPOSED QCA-BASED C-ELEMENT STRUCTURES

Figure 5a shows the proposed 2-Input QCA-based C-element structure. The simplest structure is mainly composed of a 3-input majority gate with a single feedback utilizing three different clock zones.

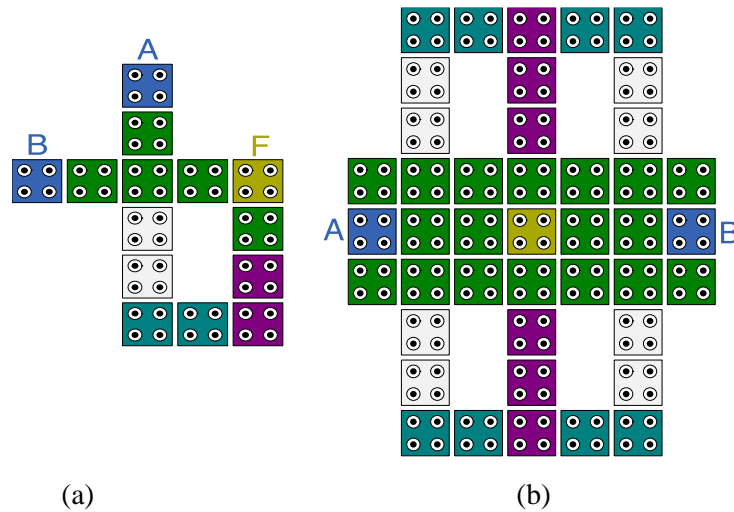


Figure 5. Proposed 2-input C-element structures: (a) Simple structure, (b) Complex structure.

As shown in Figure 5a, this structure consists of 14 cells with a total area of  $0.013\mu\text{m}^2$ . The functionality of the proposed structure can be formulated as:

$$F = \text{MAJ}(A, B, F) = A \cdot B + F \cdot (A + B) \quad (1)$$

where  $A$  and  $B$  represent the inputs and  $F$  is the output of the C-element. In this structure, the device cell is responsible for computing the majority function between the inputs ( $A$  and  $B$ ) and the output ( $F$ ), while the feedback cells are responsible for controlling the flow of information from the output ( $F$ ) to the device cell, allowing the proposed structure to achieve its intended functionality. Figure 5b shows an alternative design of the 2-input C-element, where the device cell is further duplicated to achieve a more robust design. In addition, the feedback has been duplicated to assure correct functionality in the presence of any structural defects. This design is composed of 43 cells with an area of  $0.029\mu\text{m}^2$ .

Figure 6 shows the proposed 3-input QCA-based C-element structures. Table 2 demonstrates the truth table of the 3-input C-element.

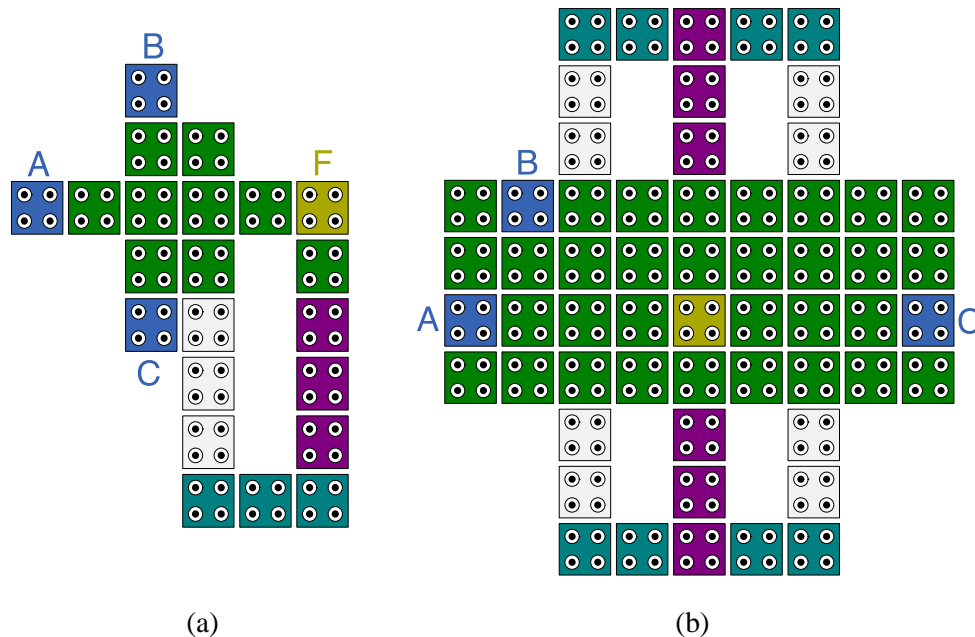


Figure 6. Proposed 3-input C-element structures: (a) Simple structure, (b) Complex structure.

Table 2. 3-Input C-element truth table.

A	B	C	$F_i$
0	0	0	0
0	0	1	$F_{i-1}$
0	1	0	$F_{i-1}$
0	1	1	$F_{i-1}$
1	0	0	$F_{i-1}$
1	0	1	$F_{i-1}$
1	1	0	$F_{i-1}$
1	1	1	1

As depicted in Figure 6a, the 3-input C-element can be implemented by modifying the simple 2-input C-element structure to accommodate more inputs while maintaining the clock zone sequence in the feedback. This design consists of 22 cells occupying an area of  $0.021 \mu\text{m}^2$ . On the other hand, Figure 6b shows a 3-input C-element structure that is achieved by modifying the design shown in Figure 5b by adding 15 more cells to accommodate an extra input while improving the robustness against structural variations.

Figure 7 illustrates the proposed 4-input C-element structures. Table 3 shows the truth table of the 4-input C-element. Figure 7a shows the simple 4-input C-element that is achieved based on a 5-input majority gate with proper structuring of the feedback. As shown, the number of used cells is 31 with an area of  $0.03\mu\text{m}^2$ . It is also possible to obtain a more robust C-element structure, as shown in Figure 7b, with a total of 67 cells.

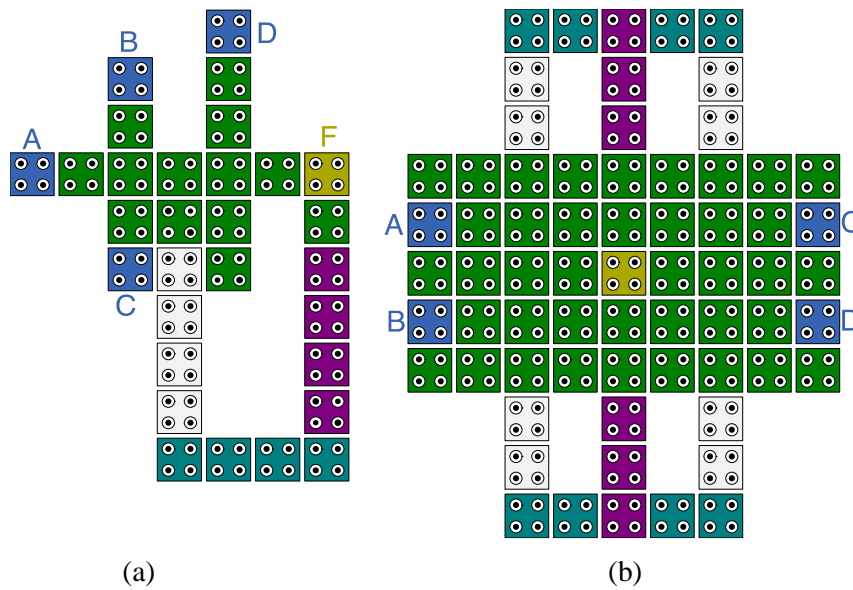


Figure 7. Proposed 4-input C-element structures: (a) Simple structure, (b) Complex structure.

Table 3. 4-Input C-element truth table.

A	B	C	D	$F_i$
0	0	0	0	0
0	0	0	1	$F_{i-1}$
0	0	1	0	$F_{i-1}$
0	0	1	1	$F_{i-1}$
0	1	0	0	$F_{i-1}$
0	1	0	1	$F_{i-1}$
0	1	1	0	$F_{i-1}$
0	1	1	1	$F_{i-1}$
1	0	0	0	$F_{i-1}$
1	0	0	1	$F_{i-1}$
1	0	1	0	$F_{i-1}$
1	0	1	1	$F_{i-1}$
1	1	0	0	$F_{i-1}$
1	1	0	1	$F_{i-1}$
1	1	1	0	$F_{i-1}$
1	1	1	1	1

### 3. RESULTS AND ANALYSIS

The QCADesigner-2.0.3 simulation tool was used to verify the functional correctness of the proposed C-element structures and assess their structural cost in terms of the occupied area [35]. The QCADesigner tool is a widely used layout and simulation tool in QCA technology to model and analyze the dynamics of QCA-based structures. In this work, simulation parameters are configured as shown in Table 4. Figures 8, 9, 10, 11, 12 and 13 show the simulation results of the proposed 2-, 3- and 4-input C-element structures, respectively under different input combinations.

As shown in Figures 8 and 9, when both inputs (A and B) are equal to (0), the output (F) is equal to (0) and maintains its logical value when one of the inputs toggles. However, when both inputs (A and B) are equal to (1), the output (F) is set to (1). Similarly, the output (F) keeps its state as long as the inputs change to distinct logical values. These observations validate the functional correctness of the proposed 2-input C-element structures. On the other hand, Figures 10, 11, 12 and 13 validate the intended functionality of the proposed 3- and 4-input structures. Apparently, the functionality of the C-element is correctly captured by the proposed structures; the output (F) only changes when the inputs have the same logic levels (0 or 1). However, when the inputs have distinct logic values, the output (F) memorizes its previous logic value.

Table 4. Simulation parameters.

Parameter	Value
Number of samples	12800
Cell Dimensions	18 nm x 18 nm
Quantum-dot diameter	5 nm
Cell separation	2 nm
Radius of effect	65 nm
Relative permittivity	12.9
Clock High	$9.8 \times 10^{-22}$
Clock Low	$3.8 \times 10^{-23}$
Clock shift	0
Clock amplitude factor	2
Layer separation	11.5 nm
Temperature	1K

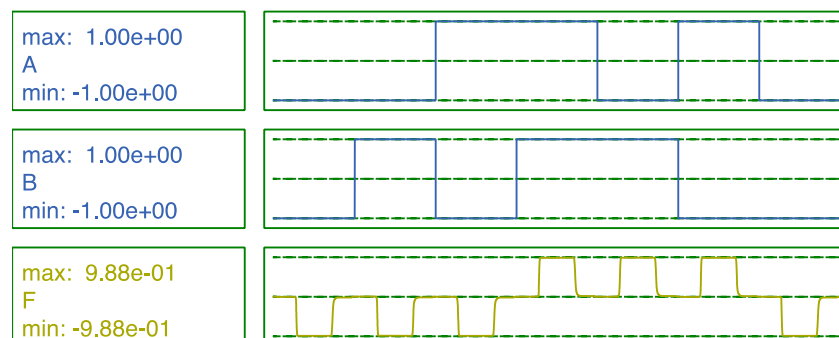


Figure 8. Simulation results of the proposed 2-input simple structure.

The only difference between simulation results of the proposed simple and complex structures is that the polarization level of the output cell (F) in the complex structures is slightly higher than that of the simple structures due to the increased level of cell interaction induced by the redundant paths to the output cell.

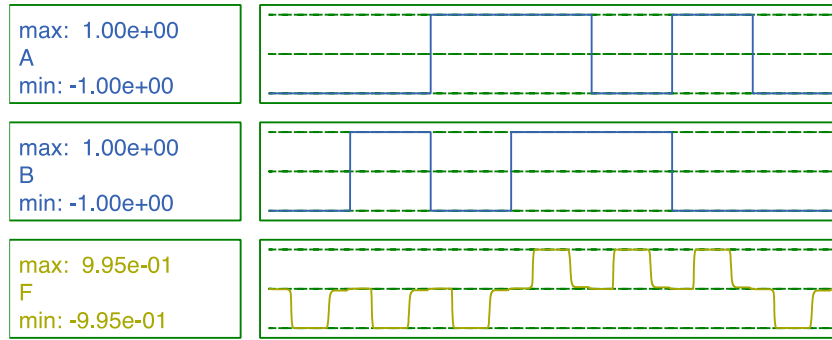


Figure 9. Simulation results of the proposed 2-input complex structure.

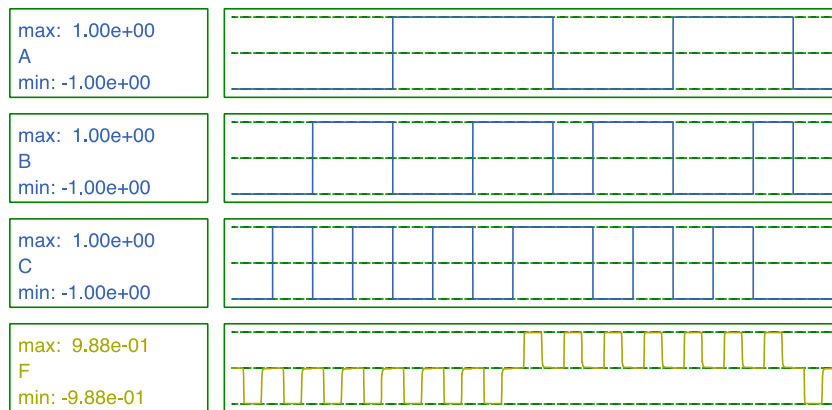


Figure 10. Simulation results of the proposed 3-input simple structure.

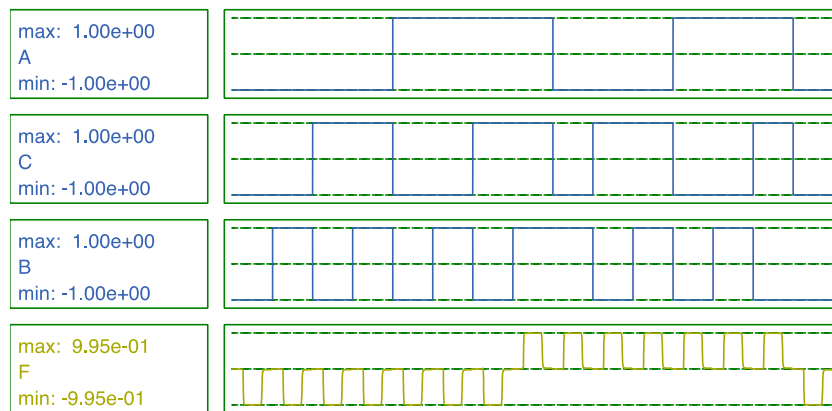


Figure 11. Simulation results of the proposed 3-input complex structure.

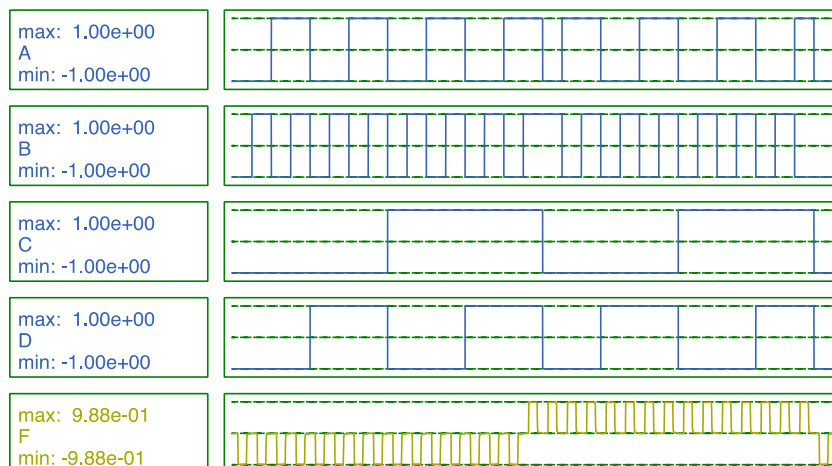


Figure 12. Simulation results of the proposed 4-input simple structure.

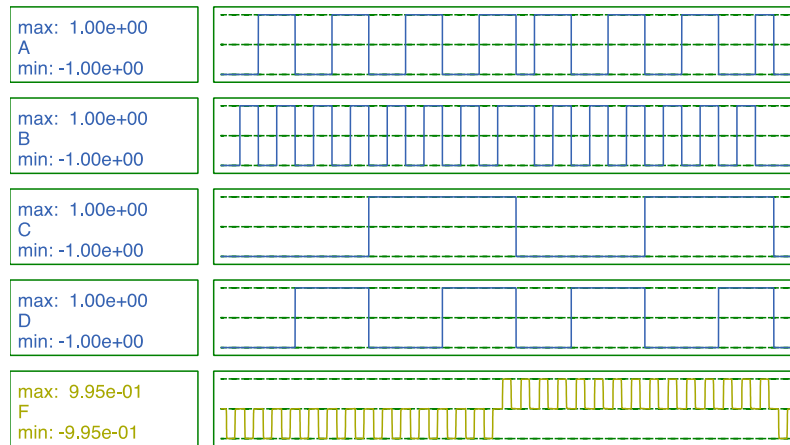


Figure 13. Simulation results of the proposed 4-input complex structure.

Figure 14 shows and compares the occupied area of the proposed C-element structures. As shown, the occupied area increases as the number of inputs is increased. In addition, the complex (i.e., with more redundant cells) structures occupy more area as compared to their simple counterparts. To estimate the energy dissipation of the various structures, the QCADesignerE tool has been used [36]. The QCADesignerE is a viable tool that models and estimates energy dissipation of QCA-based structures. Figures 15a and 15b illustrate the total energy dissipation and the average energy dissipation per clock cycle of the proposed C-element structures.

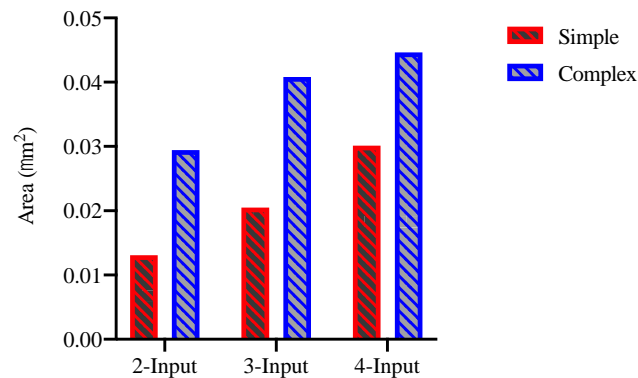


Figure 14. Area comparison of the proposed structures.

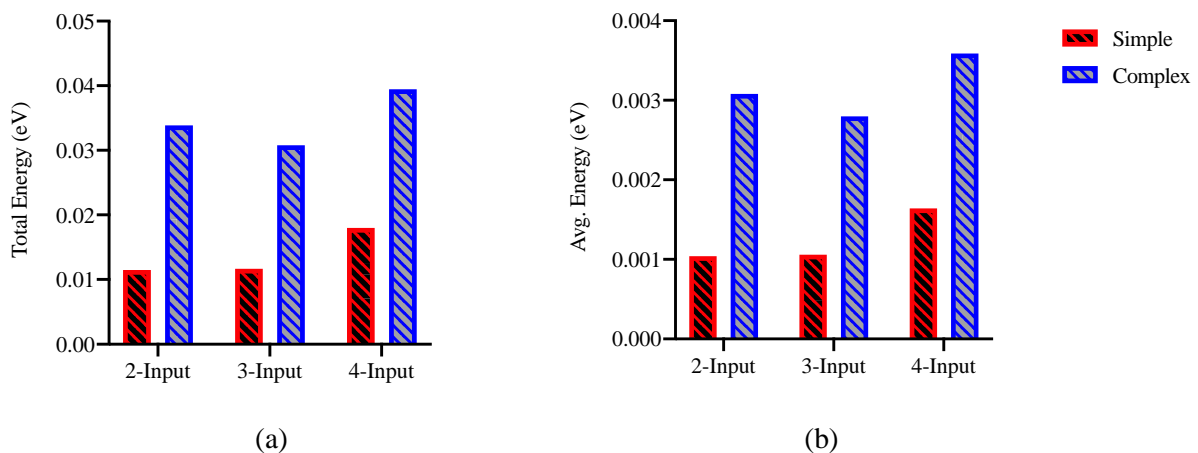


Figure 15. Energy dissipation of the proposed structures: (a) Total energy, (b) Average energy.

In order to evaluate the robustness of the proposed C-element structures, the QCADesigner-FS simulator has been used [37]. The QCADesigner-FS is a modified version of the QCADesigner tool with a capability of simulating the behavior of QCA-based structures under different structural defects. The



rationale behind this simulator is to inject a particular defect into the structure (Vacancy, Interstitial, Dopant or Dislocation) and compare the output of the defective structure to that of the defect-free structure. The structure is said to be error-free if its output in the presence of a defect matches its correct output. This process is repeated for an adequate number of simulations. The robustness of a design is quantified in terms of the percent of the error-free simulations from the total number of simulations. Figure 16 demonstrates the robustness of the various designs under different structural defects.

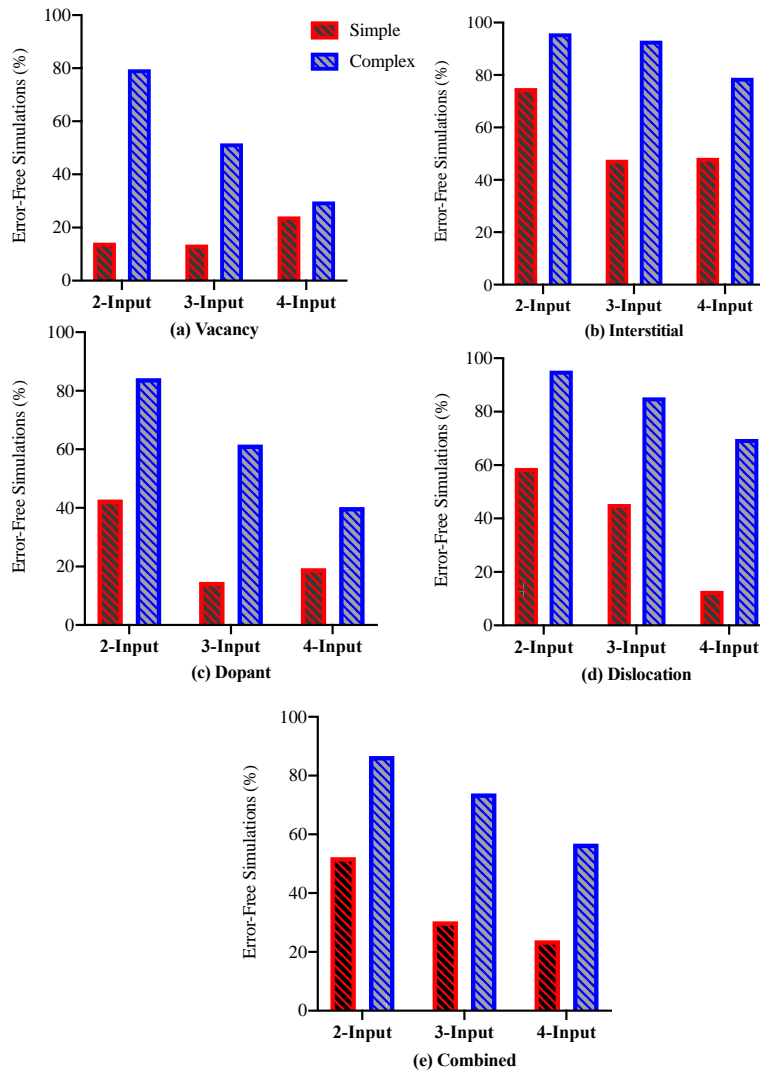


Figure 16. Robustness analysis of the proposed structures.

In Figure 16a, the robustness analysis is carried out under the vacancy (i.e., cell missing) structural defect. As shown, the proposed complex structures have higher robustness when compared to their simple counterparts. On the other hand, Figure 16b compares the robustness against interstitial defects for both simple and complex structures. It can be seen that the complex structures exhibit higher immunity against interstitial defects as compared to the simple ones. Similar trends can be observed for the dopant and dislocation structural defects, as shown in Figure 16c and 16d, respectively. Figure 16e shows the robustness analysis results under combined structural defects. The observations that can be drawn from this figure are two-fold. First, the robustness of the simple structures as well as the complex structures decreases as the number of inputs of the C-element is increased. Second, the percentages of enhancement achieved by the complex C-element structures as compared to their simple counterparts are 66%, 143% and 137% for the 2-, 3- and 4-input structures, respectively. Table 5 summarizes and compares the proposed structures in terms of cell count, area and energy dissipation, while Table 6 compares their robustness under different structural defects.

Table 5. Comparison of the proposed structures in terms of cell count, area and energy dissipation.

Structure	Inputs	Cell count	Area ( $\mu\text{m}^2$ )	Total Energy (eV)	Average Energy (eV)
Simple	2	14	0.013	1.15e-002	1.04e-003
	3	22	0.021	1.17e-002	1.06e-003
	4	31	0.030	1.80e-002	1.64e-003
Complex	2	43	0.029	3.39e-002	3.08e-003
	3	58	0.041	3.08e-002	2.80e-003
	4	67	0.045	3.95e-002	3.59e-003

Table 6. Comparison of the proposed structures in terms of robustness against different structural defects.

Structure	Inputs	Vacancy (%)	Interstitial (%)	Dopant (%)	Dislocation (%)	Combined (%)
Simple	2	14.29	75.00	42.86	58.93	52.23
	3	13.64	47.73	14.77	45.45	30.40
	4	24.19	48.39	19.35	12.90	23.96
Complex	2	79.65	95.93	84.30	95.35	86.63
	3	51.72	93.10	61.64	85.34	73.92
	4	29.85	78.95	40.30	69.78	56.83

It is worth noting that the simple structures provide easier reachability to the output cell while suffering from low immunity against structural defects. On the other hand, the complex structures achieve higher immunity against structural defects at the expense of requiring either coplanar or multilayer crossover wiring techniques to reach the output cell [38]-[39]. Moreover, the proposed QCA-based C-element structures have significant improvements in terms of area and energy dissipation as compared to previously reported CMOS-based C-element designs [40].

#### 4. CONCLUSION

In this paper, 2-, 3- and 4-input QCA-based C-element structures were proposed and evaluated in terms of their functional correctness, area, energy dissipation and robustness against structural defects. The proposed structures can be classified as either simple or complex designs. Whereas simple structures have resulted in lower area and energy dissipation with up to 56% and 66% improvement, respectively, complex ones have shown significant immunity against structural defects and achieved up to 143% improvement when compared to simple structures. In addition, the number of inputs has a pronounced impact on the considered evaluation parameters. Ultimately, the proposed structures can serve as a basis for further research in the asynchronous circuits design.

#### REFERENCES

- [1] N. B. Bousari, M. K. Anvarifard and S. Haji-Nasiri, "Improving the Electrical Characteristics of Nanoscale Triple-gate Junctionless Finfet Using Gate Oxide Engineering," *AEU International Journal of Electronics and Communications*, vol. 108, pp. 226 – 234, 2019.
- [2] A. Razavieh, P. Zeitzoff and E. J. Nowak, "Challenges and Limitations of CMOS Scaling for FinFet and Beyond Architectures," *IEEE Transactions on Nanotechnology*, vol. 18, pp. 999–1004, 2019.
- [3] W. Sung and Y. Li, "DC/AC/RF Characteristic Fluctuations Induced by Various Random Discrete Dopants of Gate-all-around Silicon Nanowire N-MOSFETs," *IEEE Transactions on Electron Devices*, vol. 65, no. 6, pp. 2638–2646, June 2018.
- [4] D. E. Nikonov and I. A. Young, "Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 1, pp. 3–11, 2015.
- [5] N. K. Chaubey and B. B. Prajapati, "Quantum Cryptography and the Future of Cyber Security," Hershey, PA, USA, pp. 1–343, 2020.

- [6] B. Debnath, J. C. Das, D. De, S. P. Mondal, A. Ahmadian, M. Salimi and M. Ferrara, "Security Analysis with Novel Image Masking Based Quantum-dot Cellular Automata Information Security Model," *IEEE Access*, vol. 8, pp. 117 159–117 172, 2020.
- [7] C. S. Lent, P. D. Tougaw, W. Porod and G. H. Bernstein, "Quantum Cellular Automata," *Nanotechnology*, vol. 4, no. 1, pp. 49–57, Jan. 1993.
- [8] H. Adepuand and I. S. Rao, "Quantum-dot Cellular Automata Technology for High-speed High-data-rate Networks," *Circuits, Systems and Signal Processing*, vol. 38, no. 11, pp. 5236–5252, Nov. 2019.
- [9] H. M. H. Babu, *Quantum Computing: A pathway to quantum logic design*, IOP Publishing, [Online], Available: <http://dx.doi.org/10.1088/978-0-7503-2747-3>, 2020.
- [10] M. Gao, J. Wang, S. Fang, J. Nan and L. Daming, "A New Nano Design for Implementation of a Digital Comparator Based on Quantum-dot Cellular Automata," *International Journal of Theoretical Physics*, May 2020.
- [11] A. N. Bahar and K. A. Wahid, "Design and Implementation of Approximate DCT Architecture in Quantum-dot Cellular Automata," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, pp. 1–10, (Early Access), 2020.
- [12] Z. Song, G. Xie, X. Cheng, L. Wang and Y. Zhang, "An Ultra-low Cost Multilayer RAM in Quantum-dot Cellular Automata," *IEEE Transactions on Circuits and Systems II: Express Briefs*, (Early Access), pp. 1–1, 2020.
- [13] M. Goswami, A. Mondal, M. H. Mahalat, B. Sen and B. K. Sikdar, "An Efficient Clocking Scheme for Quantum-dot Cellular Automata," *International Journal of Electronics Letters*, vol. 8, no. 1, pp. 83–96, 2020.
- [14] R. Laajimi, "Nanoarchitecture of Quantum-dot Cellular Automata (QCA) Using Small Area for Digital Circuits," Chapter 3 in *Book: Advanced Electronic Circuits-Principles, Architectures and Applications on Emerging Technologies*, IntechOpen, 2018.
- [15] M. Raj, L. Gopalakrishnan and S.-B. Ko, "Design and Analysis of Novel QCA Full Adder-subtractor," *International Journal of Electronics Letters*, vol. 0, no. 0, pp. 1–14, [Online], Available: <https://doi.org/10.1080/21681724.2020.1726479>, 2020.
- [16] A. H. Majeed, M. S. B. Zainal, E. Alkaldy and D. M. Nor, "Full Adder Circuit Design with Novel Lower Complexity XOR Gate in QCA Technology," *Transactions on Electrical and Electronic Materials*, vol. 21, no. 2, pp. 198–207, Apr. 2020.
- [17] D. Abedi and G. Jaberipur, "Decimal Full Adders Specially Designed for Quantum-dot Cellular Automata," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 1, pp. 106–110, 2018.
- [18] G. Cocorullo, P. Corsonello, F. Frustaci and S. Perri, "Design of Efficient BCD Adders in Quantum-dot Cellular Automata," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 5, pp. 575–579, 2017.
- [19] L. Xingjun, S. Zhiwei, C. Hongping and M. R. J. Haghighi, "A New Design of QCA-based Nanoscale Multiplexer and Its Usage in Communications," *International Journal of Communication Systems*, vol. 33, no. 4, p. e4254, 2020.
- [20] J.-C. Jeon, "Designing Nanotechnology QCA–multiplexer Using Majority Function-based NAND for Quantum Computing," *The Journal of Supercomputing*, DOI: <https://doi.org/10.1007/s11227-020-03341-8>, May 2020.
- [21] T. N. Sasamal, A. K. Singh and A. Mohan, "Design of Registers and Memory in QCA," *Proc. of the Quantum-dot Cellular Automata Based Digital Logic Circuits: A Design Perspective, Part of the Studies in Computational Intelligence Book Series*, vol. 879, pp 119-137, Springer, 2020.
- [22] A. Sadhu, K. Das, D. De and M. R. Kanjilal, "Area-delay-energy Aware SRAM Memory Cell and m x n Parallel Read/write Memory Array Design for Quantum-dot Cellular Automata," *Microprocessors and Microsystems*, vol. 72, p. 102944, 2020.
- [23] M. Patidar and N. Gupta, "An Efficient Design of Edge-triggered Synchronous Memory Element Using Quantum-dot Cellular Automata with Optimized Energy Dissipation," *Journal of Computational Electronics*, vol. 19, no. 2, pp. 529–542, Jun. 2020.

"C-Element Design in Quantum Dot Cellular Automata", M. Al-Tarawneh and Z. A. Altarawneh.

- [24] A. N. Bahar and K. A. Wahid, "Design of an Efficient  $n \times n$  Butterfly Switching Network in Quantum-dot Cellular Automata (QCA)," *IEEE Transactions on Nanotechnology*, vol. 19, pp. 147–155, 2020.
- [25] A. N. Bahar and K. A. Wahid, "Design of QCA-serial Parallel Multiplier (QSPM) with Energy Dissipation Analysis," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 10, pp. 1939–1943, 2020.
- [26] R. Marshal, G. Lakshminarayanan, S. B. Ko, N. Naganathan and N. Ramasubramanian, "Configurable Logic Blocks and Memory Blocks for Beyond CMOS FPGA Based Embedded Systems," *IEEE Embedded Systems Letters*, pp. 1–1, 2020.
- [27] S.-S. Ahmadpour, M. Mosleh and S. Rasouli Heikalabad, "Robust QCA Full-adders Using An Efficient Fault-tolerant Five-input Majority Gate," *International Journal of Circuit Theory and Applications*, vol. 47, no. 7, pp. 1037–1056, 2019.
- [28] Z. Tabassam, S. R. Naqvi, T. Akram, M. Alhussein, K. Aurangzeb and S. A. Haider, "Towards Designing Asynchronous Microprocessors: From Specification to Tape-out," *IEEE Access*, vol. 7, pp. 33978–34003, 2019.
- [29] B. Sparkman, S. C. Smith and J. Di, "Built-in Self-test for Multi-threshold Null Convention Logic Asynchronous Circuits," *Proc. of the 38<sup>th</sup> IEEE VLSI Test Symposium (VTS)*, pp. 1–6, San Diego, USA, 2020.
- [30] A. Motaqi, M. Helaloui, S. Aghli Moghaddam and M. R. Mosavi, "Detailed Implementation of Asynchronous Circuits on Commercial FPGAs," *Analog Integrated Circuits and Signal Processing*, vol. 103, no. 3, pp. 375–389, Jun. 2020.
- [31] R. Ezz Eldin, M. A. El Moursy and H. F. A. Hamed, "Synchronous and Asynchronous NoC Design Under High Process Variation," *Analysis and Design of Network-on-Chip under High Process Variation*, Cham: Springer International Publishing, pp. 71–86, 2015.
- [32] J. Spars and S. Furber, *Principles of Asynchronous Circuit Design: A Systems Perspective*, 1<sup>st</sup> Ed., Springer Publishing Company, Incorporated, 2010.
- [33] A. Yakovlev, K. Gardiner and A. Bystrov, "A C-element Latch Scheme with Increased Transient Fault Tolerance for Asynchronous Circuits," *Proc. of the 13<sup>th</sup> IEEE International On-Line Testing Symposium (IOLTS 07)*, pp. 223–230, Los Alamitos, CA, USA, 2007.
- [34] A. de Gennaro, D. Sokolov and A. Mokhov, "Design and Implementation of Reconfigurable Asynchronous Pipelines," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 6, pp. 1527–1539, 2020.
- [35] K. Walus, T. J. Dysart, G. A. Jullien and R. A. Budiman, "QCADesigner: A Rapid Design and Simulation Tool for Quantum-dot Cellular Automata," *IEEE Transactions on Nanotechnology*, vol. 3, no. 1, pp. 26–31, 2004.
- [36] F. Sill Torres, R. Wille, P. Niemann and R. Drechsler, "An Energy-aware Model for the Logic Synthesis of Quantum-dot Cellular Automata," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems*, vol. 37, no. 12, pp. 3031–3041, 2018.
- [37] D. Reis and F. Sill Torres, "A Defects Simulator for Robustness Analysis of QCA Circuits," *Journal of Integrated Circuits and Systems*, vol. 11, pp. 86–96, Aug. 2016.
- [38] M. Raj and L. Gopalakrishnan, "Cost Efficient Subtractor Designs in QCA," *Proc. of the International Conference on Electronics and Sustainable Communication Systems (ICESC)*, pp. 1168–1172, Coimbatore, India, 2020.
- [39] J. Maharaj and S. Muthurathinam, "Efficient Majority Logic Subtractor Design Using Multilayer Crossover in Quantum-dot Cellular Automata," *Journal of Nanophotonics*, vol. 14, no. 3, pp. 1 – 10.
- [40] N. Soufi and S. C. Smith, "Analysis and Design of CMOS Resettable C-elements," *Proc. of the 60<sup>th</sup> IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 104–107, Boston, USA, 2017.

**ملخص البحث:**

إنّ الطلب المستمر في السوق على أنظمة حاسوبية عالية الأداء وفعالية من حيث استهلاك الطاقة كان من شأنه أن يقود التقنيات الحاسوبية في اتجاه آليات التشغيل الذاتي الخلوية المستندة على النقط الكمية (QCA) في نطاق تكنولوجيا النانو.

تقدم هذه الورقة بنى جديدة لعنصر سي (بسيطة ومعقدة) قائمة على آليات التشغيل الذاتي الخلوية المستندة على النقط الكمية. وقد تم تحليل البنى المقترحة بالتفصيل بناءً على متغيرات تصميمية أساسية، مثل: المساحة، واستهلاك الطاقة، والحصانة ضد العيوب النيووية.

وقد أظهرت نتائج المحاكاة أن البنى البسيطة المقترحة حققت تحسناً وصل إلى ما نسبته 56% و 66% فيما يتصل بالمساحة واستهلاك الطاقة، على الترتيب. من جهة أخرى، أظهرت البنى المعقدة المقترحة حصانة راسخة ضد العيوب النيووية، محققة تحسناً وصل إلى 143% مقارنة بالبنى البسيطة. ويمكن النظر إلى بنى عنصر سي المقترحة بوصفها وحدات مهمة نافعة للتصاميم غير المترامنة.



This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).