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ARBITER DESIGN BASED ON QUANTUM DOT CELLULAR AUTOMATA

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ABSTRACT

The development of nano-scale Quantum-dot Cellular Automata (QCA) has been driven by the immense need for high-performance and energy-efficient computational systems. In this paper, 2- and 3-input QCA-based asynchronous arbiter designs are presented and investigated. A number of 2-input arbiter structures are introduced and compared with their majority-based counterpart. Simulation results show that the proposed structures outperform the majority-based arbiters in terms of number of cells, area and energy dissipation while achieving similar arbitration functionality. In addition, efficient resource utilization is obtained by configuring the proposed structures to consider the input priorities when making arbitration decision. Moreover, two 3-input arbiters are designed based on the proposed 2-input structures and proved to achieve the intended arbitration functionality. The proposed 3-input structures have surpassed their majority-based counterpart. Ultimately, the proposed arbiter designs can serve as basic building blocks in handling resource sharing in system-on-chip (SoC).

KEYWORDS

QCA, System-on-chip, Arbiter, Resource utilization.

1. INTRODUCTION

Recently, a considerable importance has been given to System-on-Chip (SoC) designs in both research and industry, as they provide significant advantages for power-efficient, high-performance computing systems [1]-[3]. Typically, an SoC is constructed by integrating several system components, such as processors, programmable logic and on-chip memories on a single chip [4]. In such systems, the most popular clocking schemes used to coordinate data transfer between different processing elements are synchronous and asynchronous schemes [5]. In synchronous clocking scheme, the clock signal serves as a global timing reference for communicating data among different modules. It synchronizes the data processing elements to manage all latches and ensure correct timing in synchronous designs. However, the modern systems contain several communication systems (or cores) on a single chip on a larger scale. In such systems, driving multiple individual cores by a single clock becomes an increasingly complicated task, which has led to the creation of cores which are asynchronous to each other. In this regard, one possible solution is to adopt asynchronous clocking scheme, where the communication channel between different cores is considered as a shared resource between the mutually competing asynchronous subsystems. A dedicated arbitration circuit (or arbiter) is used to provide access to one or more shared resources, such as memory, difficult data processors or channels of communication. A fundamental illustration of arbitration process: suppose two transmitters that require to send data over a common network connection (channel). They cannot use the channel at the same time, so they are requesting a dedicated arbiter to approve access to the shared resource. The arbiter in turn ensures that the resource is available before access is granted to any of them.

Many research efforts have focused on the design and optimization of arbiters based on conventional CMOS technology [6]-[11]. However, with the rapid development of CMOS technology reaching the nanoscale limits, some issues, like power consumption and increased leakage current, are becoming a major impediment for further improvement in device scaling. According to the International Technology Roadmap for Semiconductors (ITRS) projections, the development of new device technologies is inevitable in future technology nodes [12]-[13]. In this regard, the nanoscale Quantum-dot Cellular Automata (QCA) technology is anticipated to offer higher density, lower power consumption and more flexible interconnection designs for future SoC. The binary values in the QCA-based elements depend on the positions of confined electrons in carefully designed quantum dots, allowing QCA-based designs to outperform CMOS-based designs in terms of switching speed, device density and power consumption

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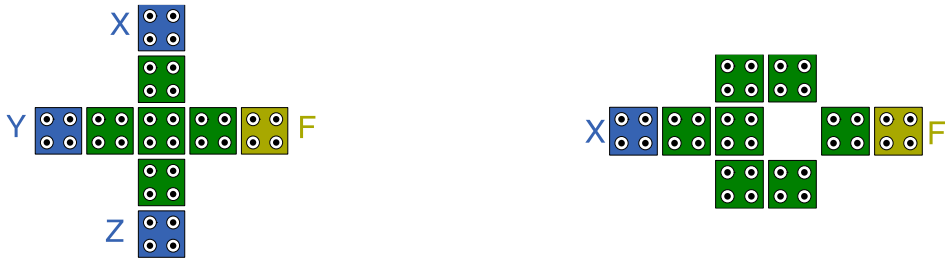
[14]-[15]. Typically, all computational logic gates and memory structures can be designed by assembling QCA cells in specific geometric patterns to achieve the intended functionality [16]-[17]. In QCA technology, the majority and inverter gates are the basic building blocks to synthesize different circuits. These gates are depicted in Figure 1. Other primitive logic gates, such as AND and OR logic gates, can be implemented based on the 3-input majority gate by fixing one of the inputs to either ”0” or ”1”, respectively.



(a) (b)

Figure 1. Basic QCA building blocks: (a) Majority gate. (b) Inverter.

In QCA circuits, switching from one binary state to another is achieved by using external clock signals that control the inter-dot tunneling barriers, allowing the transfer of electrons between dots [18], as shown in Figure 2. In order to obtain stable logic states and information flow between adjacent cells, the inter-dot barrier of QCA cells is appropriately controlled through four different clock phases; namely, switch, hold, release and relax [18]-[19]. During the switch phase, a cell begins unpolarized and the inter-dot barrier is slowly raised and pushes the electrons into the corner dots, allowing it to attain a definitive polarity under the influence of its neighbors (which are in the hold phase). In the hold phase, barriers are held high and a cell maintains its polarity and acts as input to the neighboring cells. During the release phase, the potential barrier is slowly lowered until the cell loses its polarity. In the last phase; namely, relax, the barriers remain lowered and keep the cell in an unpolarized state, as shown in Figure 2. In addition, the QCA cells in a particular design are typically divided into sequential clocking zones whose clock signals are shifted by 90 degrees to synchronize polarization changes throughout QCA-based structures besides preventing back-propagation of information between adjacent cells.

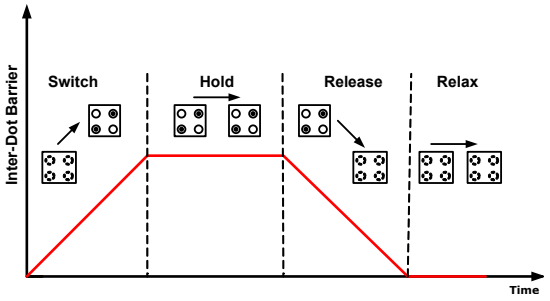


Figure 2. Inter-dot barrier in different clock phases.

In the last few years, significant research efforts have been made on the design of various SoC structures and their related interconnection networks, such as nano-router [20]-[23], serial communication network [24], error detection and correction systems [25] based on QCA technology. More recently, the authors of [26] have proposed various designs of QCA-based nano-arbiters, including the round-robin and the ping-pong arbiters, which are considered as synchronous arbiters. The proposed designs were implemented by translating the existing CMOS-based designs into equivalent majority-based QCA circuits, which ultimately could increase circuit complexity and power dissipation. However, to the best of our knowledge, no previous designs related to QCA-based asynchronous arbiters are reported in literature. This paper presents various implementations of 2- and 3-input QCA-based asynchronous arbiters. The proposed designs rely on cell interactions to achieve the intended functionally while reducing circuit complexity. Several designs were proposed based on a common baseline to overcome

the metastability issue and introduce the notion of priority in the arbitration process. Finally, the proposed designs were simulated and analyzed to verify their functionality and assess their performance metrics. Ultimately, the proposed structures can serve as fundamental components in building large-scale, static-priority multi-way arbiters.

The rest of this paper is organized as follows. Section 2 shows the proposed arbiter structures. Section 3 presents simulation results and compares the proposed structures in terms of their area and energy dissipation. Finally, section 4 summarizes and concludes.

2. PROPOSED QCA-BASED ARBITER STRUCTURES

Figure 3 shows a majority-based QCA 2-input arbiter which implements the functionality characterized in Equation 1. The majority-based design consists of 36 QCA cells. As shown, the majority-based design requires the QCA cells to be divided into two different clock zones (clock zone 0 and clock zone 1) in order to achieve the proper functionality shown in Table 1.

$$G1 = MAJ(R1, NOT(R2), 0) = R1.\overline{R2}$$
$$G2 = MAJ(NOT(R1), R2, 0) = \overline{R1}.R2 \quad (1)$$

where R1 and R2 represent the input requests while, G1 and G2 represent the output grants.

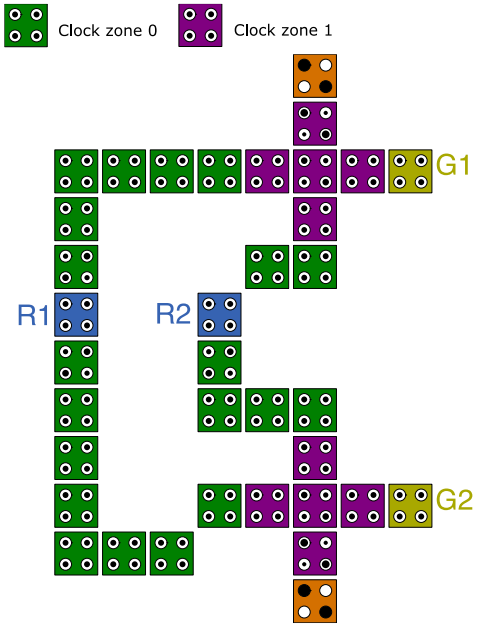


Figure 3. Majority-based 2-input arbiter.

Table 1. 2 - input majority-based arbiter truth table.

R1	R2	G1	G2
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

In fact, a key factor in characterizing an arbiter is its fairness in granting access to shared resources. Fairness is a measure of the ability of an arbiter to provide equal service to different requesters [9], [27]-[28]. As shown in Table 1, both requesters (R1 and R2) in the majority-based arbiter have equal chance of being granted access to a shared resource.

Figures 4(a) and 4(b) show the proposed baseline 2-input QCA-based arbiter structures. The first baseline structure (4(a)) is mainly composed of two L-shaped back-to-back QCA wires with two inputs (R1 and R2) and two outputs (G1 and G2). As shown, the design consists of 12 QCA cells. On the other hand, the other baseline design (4(b)) has less number of cells and is composed of 10 QCA cells.

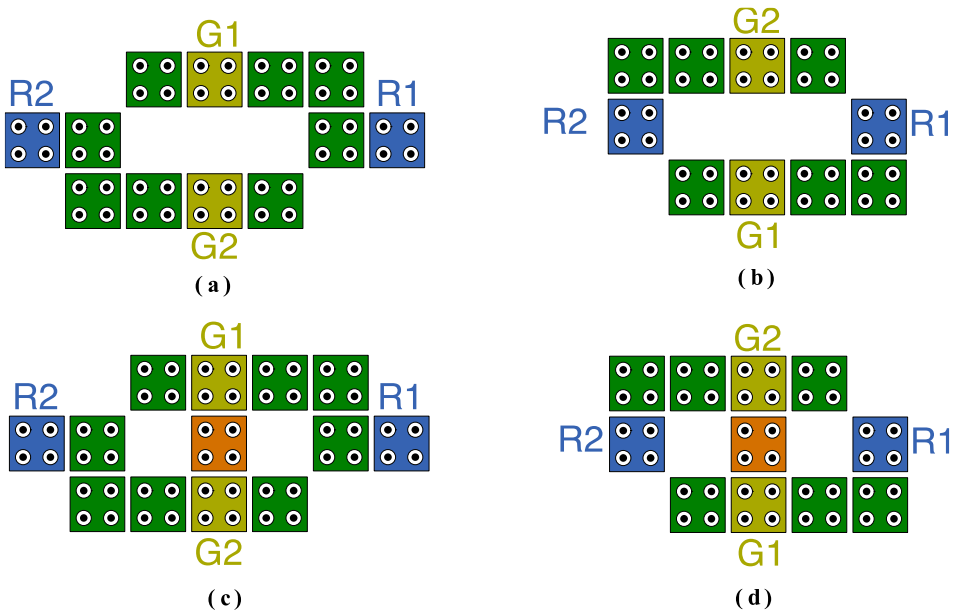


Figure 4. Proposed 2-input arbiter structures. (a) Baseline - design A, (b) Baseline-design B, (c) Modified (A) with fixed polarization (p=-0.01) and (d) Modified (B) with fixed polarization (p=-0.25).

Table 2 shows the truth table of the baseline designs. The drawback of such designs appears when the two input (request) lines are set to 0 or 1 simultaneously. As a result, a metastable state would arise, causing the output (grant) lines to potentially be activated simultaneously or grant resource access while the request line is not activated. Apparently, the occurrence of metastable states violates the concept of arbitration of resources, which dictates that only one grant line can be active at a time when a resource request is initiated. In general, the metastability phenomenon in a defect-free structure comes from unexpected polarization levels induced from the neighboring cells [29]. In the proposed baseline structures, the polarity of the output cells (G1 and G2) is determined by comparing the total electrostatic energies of two polarizations under the effect of information flow from the opposite input paths (i.e., R1 and R2). The polarization of the output cell having the smallest energy is considered to be its stable state. Due to the symmetrical cell configuration around the output cells (G1 and G2) in the proposed baseline structures, the electrostatic energies of the output cells induced from the two competing paths (from R1 and R2) are equal when both R1 and R2 have the same logic values. As a result, the output cells will be in metastable states, since the two possible polarizations, inside the output cells, will have the same energy levels. Hence, the output cells will settle in either logic 0 or 1.

Table 2. 2-input baseline arbiter truth table.

R1	R2	G1	G2
0	0	1/0	1/0
0	1	0	1
1	0	1	0
1	1	1/0	1/0

To address this issue, an extra cell with fixed polarization is introduced in the design to resolve the metastable states, as shown in Figures 4(c) and 4(d) which present other alternative 2-input arbiter designs. The addition of the fixed polarization cell with (p = -0.01) in 4(c) and (p = -0.25) in 4(d) will mitigate the metastability issue by forcing the output cells to be in logic 0 state when both R1 and R2 have the same logic values. As shown, the number of QCA cells is reduced while resolving the metastable states. The truth table of the modified 2-input arbiters is equivalent to that of the majority-based arbiter shown in table 1. It can be observed that the fairness of the modified 2-input arbiters is similar to that of the majority-based design. However, when R1 and R2 have distinct logic levels, the effect of the fixed polarization cell on the output cells is negligible due to its low polarization level, as shown in Figure 5, which shows the simulation results of the modified 2-input arbiters.

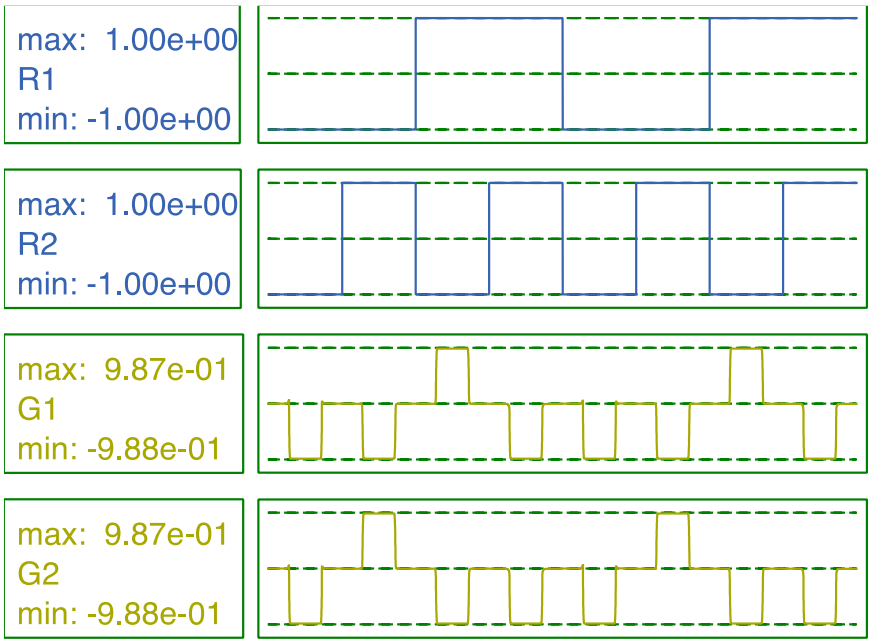


Figure 5. Simulation results of the modified 2-input arbiters.

A common theme among the modified 2-input arbiter designs is that no grants are given when both requests are issued at the same time (as shown in Figure 5) leading to a poor resource utilization. To remedy this situation, the notion of priority is introduced in order to favor one request line over the other when R1=R2=1. This can be achieved by adding 2 extra QCA cells with a fixed polarization, as shown in Figure 6. In Figure 6(a), the values of p1 and p2 were set to 0.0015 and -0.005, respectively in order to give R1 higher priority than R2. On the other hand, R2 is given higher priority than R1 by interchanging the fixed polarization values, as shown Figure 6(b). Although the introduction of priority in the arbiter design enhances resource utilization, it reduces the fairness of the proposed priority-based arbiters as compared to the majority-based and the modified 2-input arbiters. Figure 7 demonstrates the simulation results of the 2-input arbiter where input request R1 (7(a)) and input request R2 (7(b)) are given higher priority, respectively.

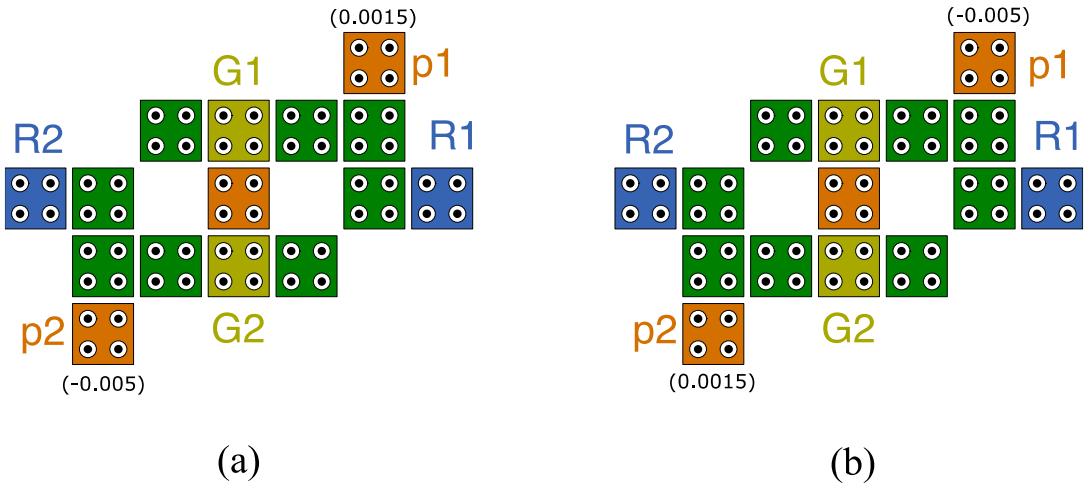


Figure 6. Priority-based 2-input arbiter structures. (a) High priority for R1 (b) High priority for R2.

Figure 8 shows a majority-based 3-input arbiter which is composed of 6 majority gates to implement the intended arbitration functionality. This structure consists of 133 QCA cells. As shown, the QCA cells in the majority- based design are assigned to four different clocking zones (i.e., clock zones 0,1,2 and 3) in order to attain the proper functionality depicted in Equation 2 and Table 3. Figure 9 depicts the simulation results of the majority-based 3-input structure.

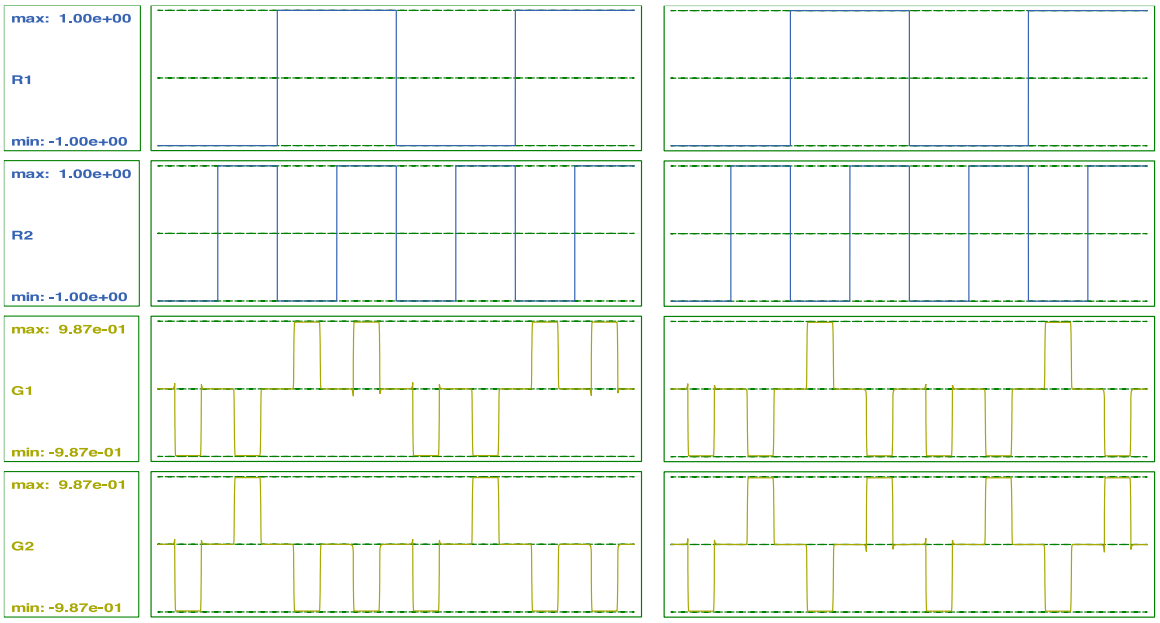


Figure 7. Simulation results of priority-based 2-input arbiter. (a) Higher priority for R_1 (b) Higher priority for R_2.

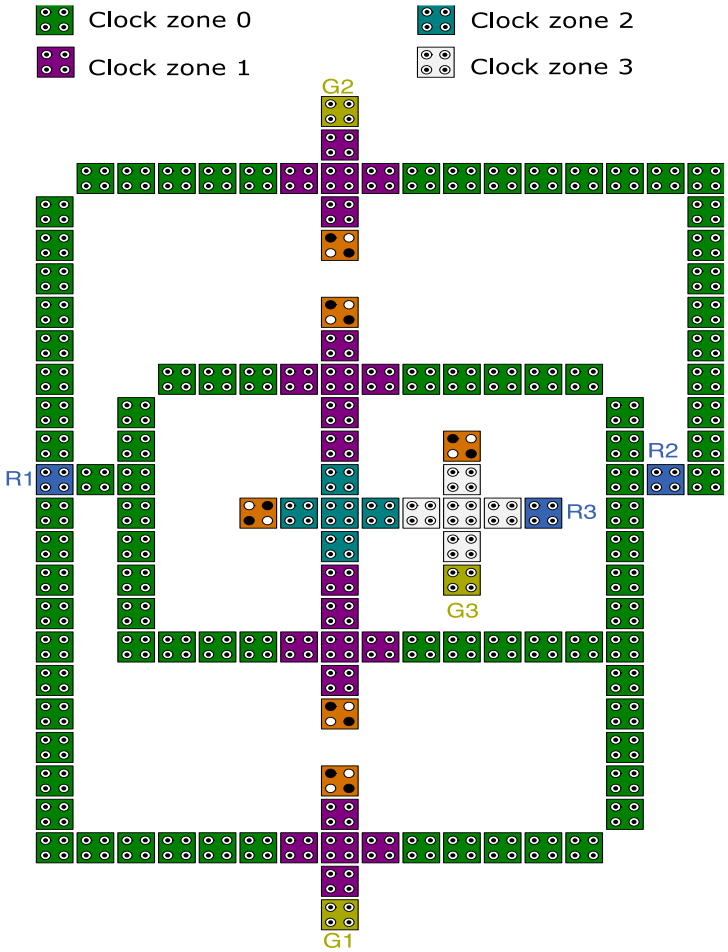


Figure 8. 3-input arbiter structure; majority-based.

$$G1 = R1.\overline{R2}.\overline{R3} + R1.\overline{R2}.R3$$
$$G2 = \overline{R1}.R2.\overline{R3} + \overline{R1}.R2.R3 \quad (2)$$
$$G3 = \overline{R1}.\overline{R2}.R3 + R1.R2.R3$$

where R1, R2 and R3 represent the input requests, while G1, G2 and G3 represent the output grants.

Table 3. Truth table of the majority-based 3-input arbiter.

R1	R2	R3	G1	G2	G3
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	0	1

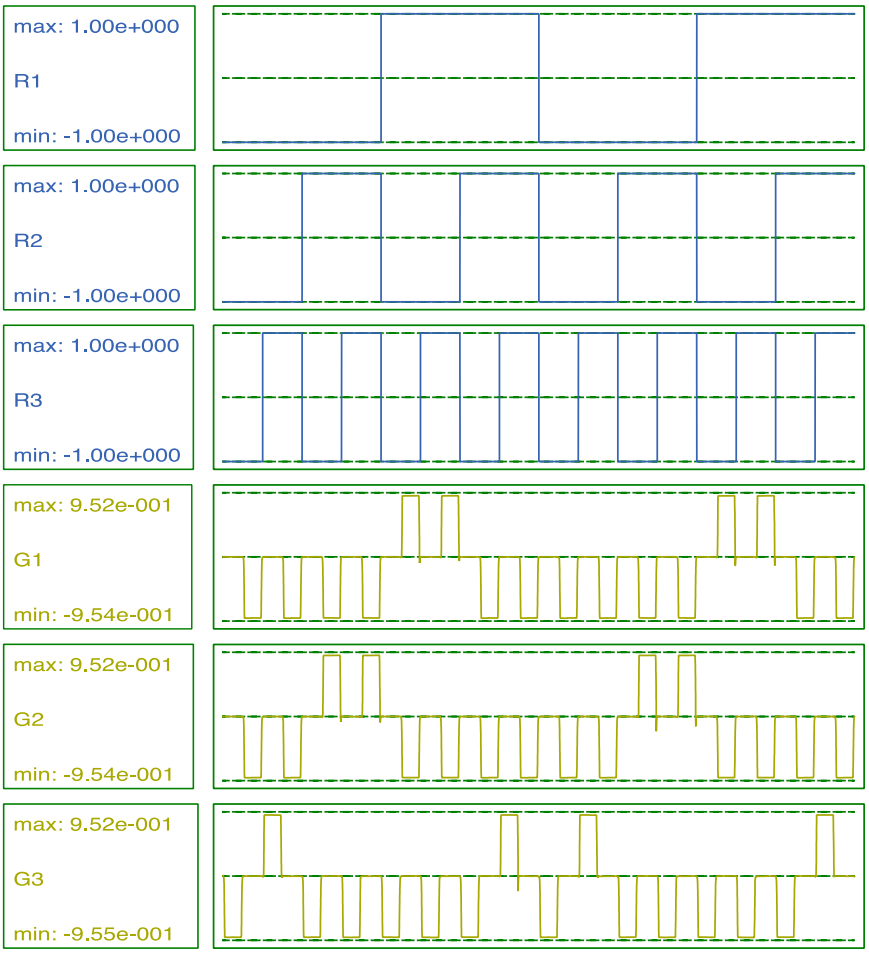


Figure 9. Simulation results of the majority-based 3-input arbiter.

Figure 10 shows an alternative design for a 3-input arbiter (Design A). This design relies on the proposed 2-input arbiters in which the arbitration functionality is achieved based on cell interactions without explicitly relying on majority gates. In Figure 10, R1 and R2 are first arbitrated using a 2-input arbiter and then combined and fed to another 2-input arbiter to which the third request line (R3) is connected.

Table 4 demonstrates the functionality of the proposed 3-input arbiter shown in Figure 10. It can be noticed that request lines R1 and R2 were given higher priority as compared to R3 except in the cases where R1 and R2 have the same logical value. For instance, when R1=R2=1, the grant line (G3) captures the value of R3 as evident in Equation 3. It can also be observed that the design shown in Figure 10 does not provide fair arbitration between requesters (i.e., R1, R2 and R3), since it assumes a static priority assignment among requesters. Figure 11 shows the simulation results of the 3-input arbiter which clearly demonstrates that the proposed design achieves mutual exclusion between request lines by ensuring that no grant lines are activated at the same time.

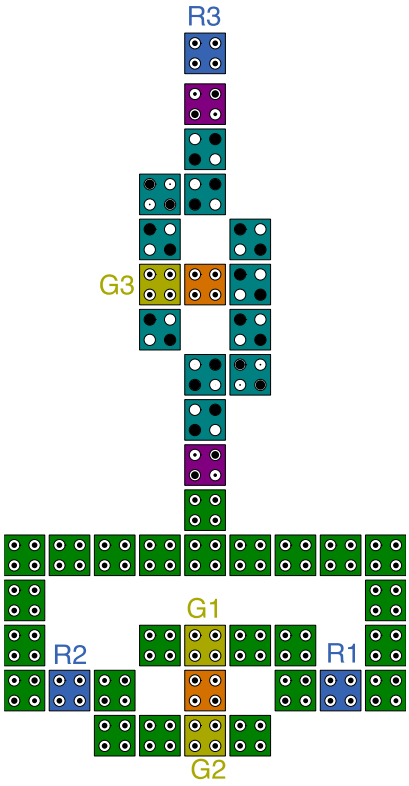


Table 4. Truth table of the 3-input arbiter (Design-A).

R1	R2	R3	G1	G2	G3
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	(1-0)	(0-1)
1	0	0	1	0	0
1	0	1	(1-0)	0	(0-1)
1	1	0	0	0	0
1	1	1	0	0	1

Figure 10. 3-input arbiter structures - Design A.

$$G1 = R1.\overline{R2}.\overline{R3} + R1.\overline{R2}.R3$$
$$G2 = \overline{R1}.R2.\overline{R3} + \overline{R1}.R2.R3 \quad (3)$$
$$G3 = \overline{R1}.\overline{R2}.R3 + \overline{R1}.R2.R3 + R1.\overline{R2}.R3 + R1.R2.R3$$

where R1, R2 and R3 represent the input requests, while G1, G2 and G3 represent the output grants.

Figure 11. Simulation results of 3-input arbiters - Design A.

Figure 12 shows a different design for the 3-input arbiter (Design B) that maintains the 3-input arbitration functionality depicted in Table 3 and Equation 2.

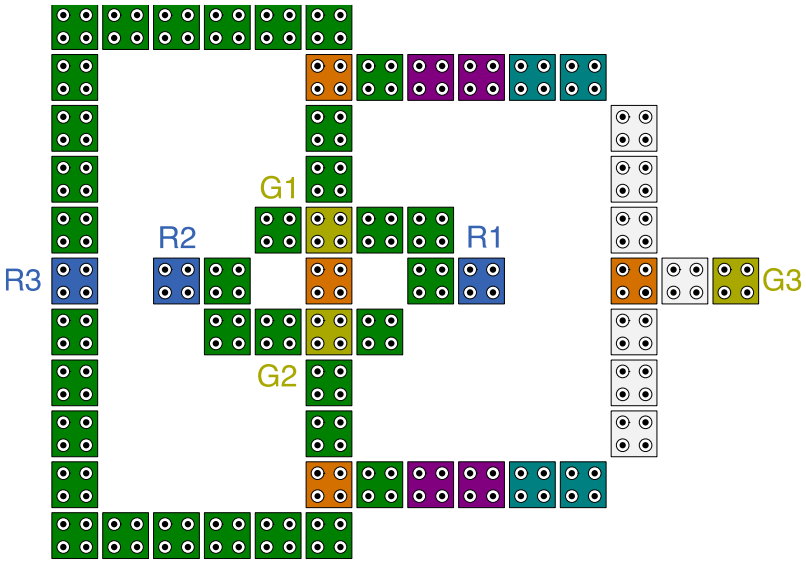


Figure 12. 3-input arbiter structures - Design B.

One of the main distinctions between the proposed 3-input arbiter designs is that the resource utilization in the design shown in Figure 10 (Design A) is better than those of the other proposed designs, as the number of resource grants is higher under the same input request combinations, as shown in Figure 13. However, the other two designs provide fair arbitration between requesters.

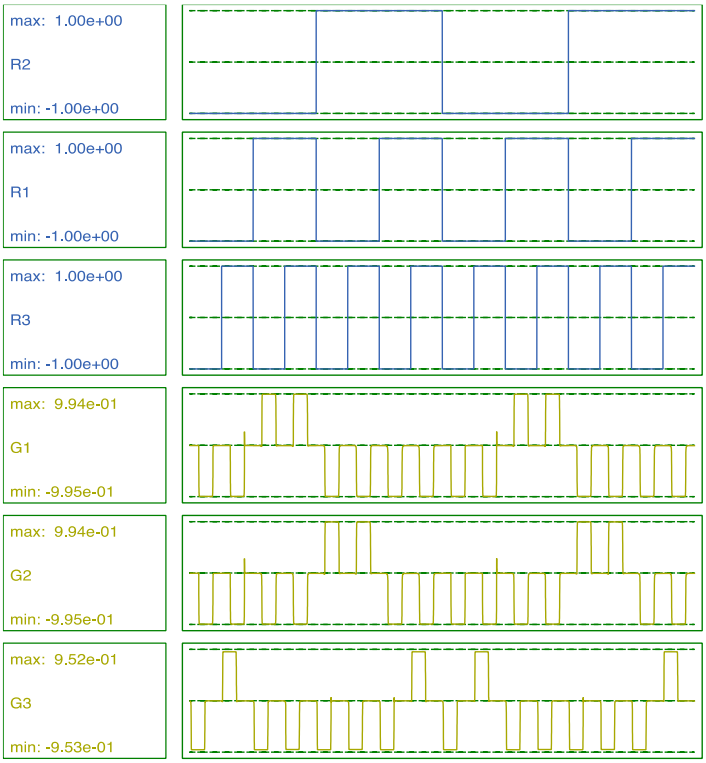


Figure 13. Simulation results of 3-input arbiters - Design B.

A more realistic implementation of the proposed 3-input structures can be obtained by adopting the two-dimensional wave (2-DW) clock distribution scheme that is based on parallel execution and processing in clocking zones [30]-[31]. The rationale behind this scheme is to overcome the limitations of the 1-D clocking scheme such as thermal fluctuation in QCA-based structures. Figures 14 and 15 show the 2-DW implementations of the proposed 3-input arbiters.

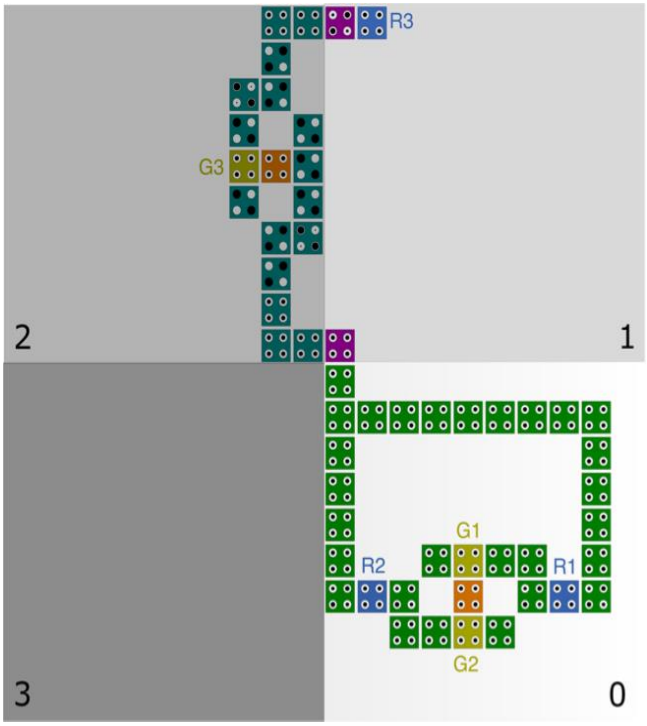


Figure 14. Realistic 2D implementation of 3-input arbiter - Design A.

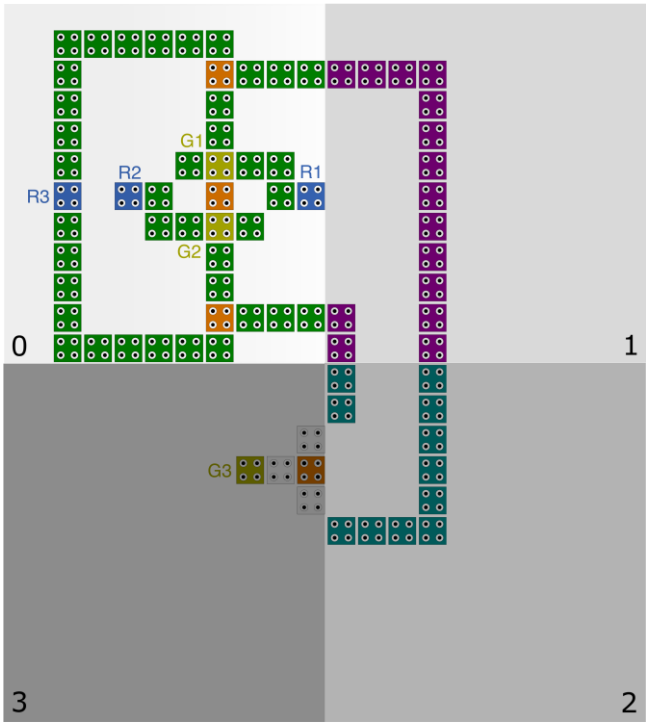


Figure 15. Realistic 2D implementation of 3-input arbiter - Design B.

3. PERFORMANCE ANALYSIS

The QCADesigner-2.0.3 simulation tool was used to analyze the proposed arbiter structures and assess their structural cost in terms of their number of cells and occupied area [32]. The QCADesigner tool is a widely used layout and simulation tool in QCA technology to model and analyze the dynamics of QCA-based structures. In this work, simulation parameters are configured as shown in Table 5.

Table 5. Simulation parameters.

Parameter	Value
Number of samples	12800
Temperature	1K
Relative permittivity	12.9
Clock high	9.8×10^{-22}
Clock low	3.8×10^{-23}
Clock shift	0
Clock amplitude factor	2
Cell dimensions	18 nm x 18 nm
Quantum dot diameter	5 nm
Cell separation	2 nm
Radius of effect	65 nm
Layer separation	11.5 nm

Figure 16 shows and compares the proposed arbiter designs in terms of the number of QCA cells required to achieve the proper functionality of the 2- and 3-input arbiters. As shown in Figure 16, all the proposed 2-input arbiters have fewer cells as compared to the majority-based 2-input structure. Moreover, the proposed 3-input arbiter structures (Design A and Design B) have lower number of cells when compared to the 3-input majority-based structure. The variation in the number of QCA cells has a noticeable consequence on the total occupied area, as shown in Figure 17. The total area is in fact the rectangular area which encapsulates all the QCA cells in a QCA-based structure including empty spaces.

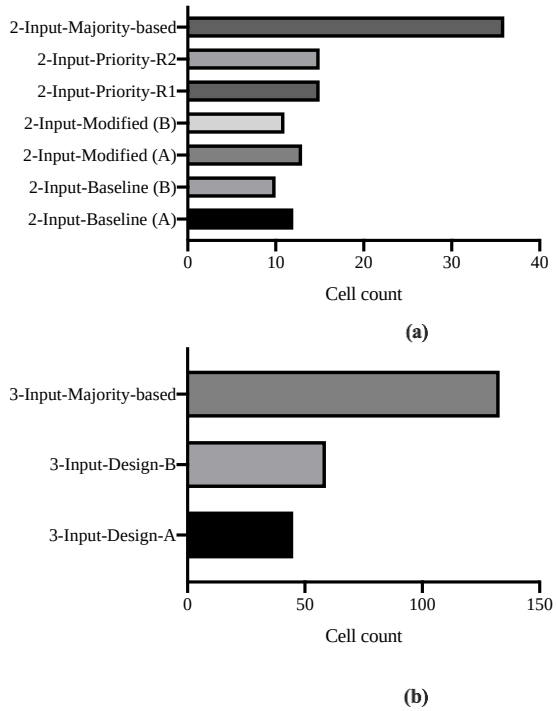


Figure 16. Number of cells comparison, (a) 2-input arbiters. (b) 3-input arbiters.

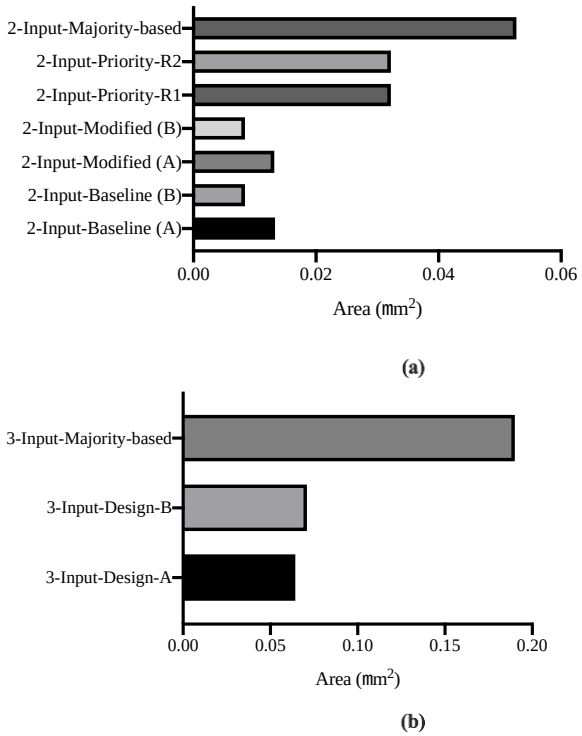


Figure 17. Occupied area comparison, (a) 2-input arbiters. (b) 3-input arbiters.

To estimate the energy dissipation of the various structures, the QCADesignerE tool has been used [33]. The QCADesignerE is a viable tool that models and estimates energy dissipation of QCA-based structures. Figures 18 and 19 illustrate the total energy dissipation and the average energy dissipation per clock cycle of the proposed arbiter structures.

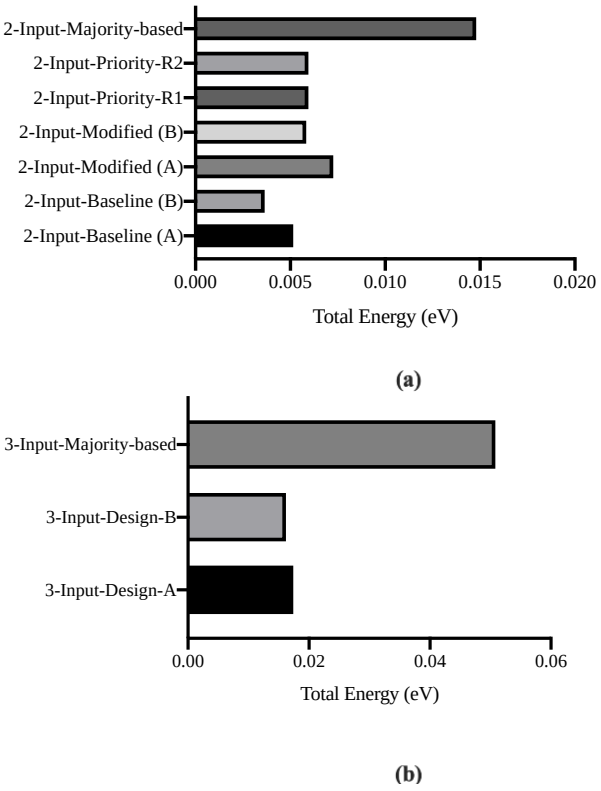


Figure 18. Total energy dissipation of the proposed structures. (a) 2-input arbiters. (b) 3-input arbiters.

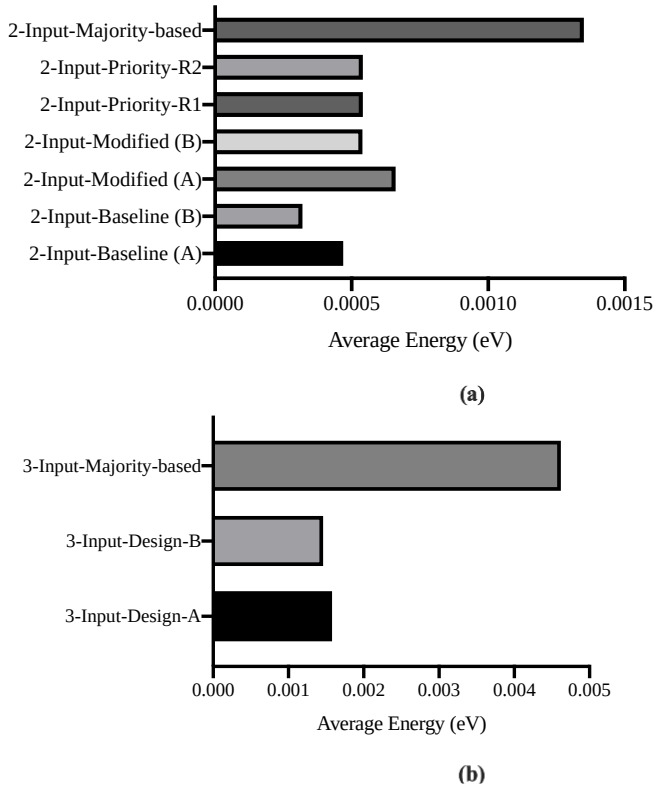


Figure 19. Average energy dissipation of the proposed structures. (a) 2-input arbiters. (b) 3-input arbiters.

For the 2-input arbiters, all of the proposed designs have less total energy dissipation and average energy per clock cycle as compared to the majority-based structure. For the 3-input arbiters, they have higher energy dissipation values as compared to the 2-input structures. In addition, the majority-based 3-input arbiter has higher energy dissipation values as compared to the other 3- input arbiters that have almost identical energy dissipation values, as shown in Figures 18 and 19. Table 6 compares the proposed 2-input arbiters against recently reported QCA-based arbiters. The comparison factors include arbiter type, cell count, area and latency. As shown, the proposed asynchronous arbiters outperform their synchronous counterparts in terms of their cell count, area and latency. The latency is defined as the number of cycles required to obtain the circuit's output after input's application. It is anticipated that the proposed 3-input arbiters would outperform synchronous designs as the 2-input structures can serve as building blocks for other large-scale arbiters.

Table 6. Comparison of the proposed structures with previous arbiter designs.

Structure	Type	Cell count	Area (μm^2)	Latency
Basic round-robin arbiter [26]	synchronous	636	1.14	5
Improved round-robin [26]		189	0.27	2
Ping pong arbiter [26]		147	0.2	2
2-input-modified	asynchronous	13	0.0131	0.25
2-input-alternative		11	0.0137	0.25
2-input-priority-based		15	0.0322	0.25
2-input-majority-based		36	0.053	0.25

4. CONCLUSION

In this paper, different QCA-based arbiter structures were presented and thoroughly evaluated. For the 2-input arbiter structures, our proposed structures outperformed the majority-based structure in terms of the number of cells, area occupation and energy dissipation. These structures can be configured to improve resource utilization by assigning different priorities for the input requests. The proposed 2-input designs were further extended to accommodate 3-input request lines. Two 3-input arbiter designs were proposed. The proposed 3-input designs were found to have fewer cells, lower area and energy dissipation as compared to their majority-based counterpart. Ultimately, the proposed 2- and 3-input structures can serve as basic building blocks in asynchronous computational systems.

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ملخص البحث:

تطورت أنظمة خلايا النّقط الكمّيّة القائمة على التّشغيل الذّاتي في مستوى النّانو بفعل الحاجة الشديدة الى أنظمة حوسبة عالية الأداء وفعّالة من حيث استهلاك الطاقة. في هذه الورقة، يتم تقديم واستقصاء أنظمة خلايا نّقط كمّيّة قائمة على التّشغيل الذّاتي، ثنائية المداخل وثلاثية المداخل. يتم اقتراح عدد من أنظمة التّحكيم ثنائية المداخل ومقارنتها بنظيرتها من الأنظمة القائمة على الأغلبية.

وتبيّن نتائج المحاكاة أنّ البِنى المقترحة تتفوّق على أنظمة التحكيم القائمة على الأغلبية من حيث عدد الخلايا، والمساحة، واستهلاك الطاقة في الوقت الذي تحقق فيه نتائج وظيفيّة مماثلة. بالإضافة الى ذلك، يتم تحقيق استغلال فعّال للمصادر عن طريق تشكيل البِنى المقترحة بحيث تأخذ الأولويات بعين الاعتبار عندما تتّخذ قرار التّحكيم.

علاوة على ذلك، تمّ تصميم اثنين من أنظمة التّحكيم ثلاثية المداخل استناداً الى البِنى ثنائية المداخل المقترحة، وقد أثبتت نجاعتها في تحقيق النّتائج الوظيفيّة المرجوة بفاعلية. وقد تفوّقت البِنى المقترحة ثلاثية المداخل على نظيرتها القائمة على الأغلبية.

وختاماً، يمكن لتصاميم أنظمة التّحكيم المقترحة أن تخدم كوحدات بناء أساسيّة للتَّعامل مع تشارُك المصادر في الأنظمة المجمّعة بكاملها على دارة متكاملة.