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DESIGN METHODOLOGY FOR NARROW-BAND LOW NOISE AMPLIFIER USING CMOS 0.18 μM TECHNOLOGY

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ABSTRACT

This paper presents a design methodology for a fully integrated narrow-band low noise amplifier (LNA). To demonstrate the effectiveness of the proposed methodology, an LNA for Wi-Fi and Bluetooth standards at 2.4 GHz is conducted. The design circuity is implemented using 0.18 µm TSMC CMOS technology; however, the methodology can be equally applied to any process node. Optimum transistor sizing and biasing to achieve minimum noise figure (NF) and maximum power gain without violating the specified power budget are attained by this methodology. It also specifies the criteria for choosing the on-chip RF inductors based on the quality factor, self-resonance frequency and area. The demonstrated LNA design achieves a power gain (S_{21}) of 22.75 dB, an input return loss (S_{11}) of –30.11 dB, a reverse isolation (S_{12}) of –60.49 dB and an output return loss (S_{22}) of –11.23 dB. The linearity parameters of the $P_{1\text{-}dB}$ compression point and IIP_3 are –19 dBm and –13.5 dBm, respectively. It produces an NF of 1.75 dB while consuming 6.16 mW from a 1.8 V power supply.

KEYWORDS

Design methodology, Front-end receiver, LNA, Wireless network, Bluetooth, IEEE 802.11 b, IEEE 802.15.1, 0.18 µm CMOS.

1. INTRODUCTION

Wi-Fi and Bluetooth are ubiquitous among almost all modern devices, as they are used to connect users to the Internet and other peripheral devices. There is a need for high-performance, low-power and low-cost devices to keep up with the customers' need for battery-operated devices. CMOS technology has been very popular in building these devices due to its superior capability of integration, low cost, low power and accessibility. The design of Wi-Fi and Bluetooth front-end receivers is challenging due to several opposing requirements. One of the main building blocks of the front-end receiver is the low noise amplifier (LNA), as it determines the noise figure (NF) and hence the overall sensitivity of the receiver.

The key performance metrics in designing the LNA include NF, power gain, linearity, input-output impedance-matching circuits, stability and reverse isolation. Indeed, all these design parameters are equally critical, but there are unavoidable trade-offs among them when attempting to build an optimum LNA [1]-[3]. Due to this complex inter-relationship among all these entities, there is a need for a simple and precise methodology to obtain optimal performance for a given LNA.

There is a wealth of prior art that has been published optimizing the design of LNA and its performance parameters using different topologies and different techniques. However, there is a lack of a simple and comprehensive design methodology that guides the RF designer through different steps, starting from a set of design specifications to the optimal design parameters [4]-[9].

This paper presents a simple, concise and comprehensive design methodology for narrow-band LNA. The proposed design methodology specifically explains the topology selection with detailed analysis. In addition, the methodology uses g_m/I_D technique to select the optimum transistor sizing and biasing to achieve minimum NF and maximum power gain without violating the specified power budget. It also specifies the criteria for choosing the on-chip RF inductors based on the quality factor, self-resonance frequency and area. Although the methodology utilized the 0.18 µm process node, it can be easily extended to any other process node.

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This paper is organized as follows: Section 2 presents the design methodology for narrow-band LNA operated at 2.4 GHz. In Section 3, the simulation results are presented and compared with those of some recently reported works. Finally, conclusions are given in Section 4.

2. DESIGN METHODOLOGY

This section depicts the proposed design methodology demonstrated with LNA for Wi-Fi and Bluetooth. The flowchart illustrated in Figure 1 summarizes the steps to be followed in designing a narrow-band LNA with optimal performance parameters. The methodology starts with the targeted design specifications and ends up with optimal design parameters. The main steps of the flow charts are given in the following sub-section and Section 3.

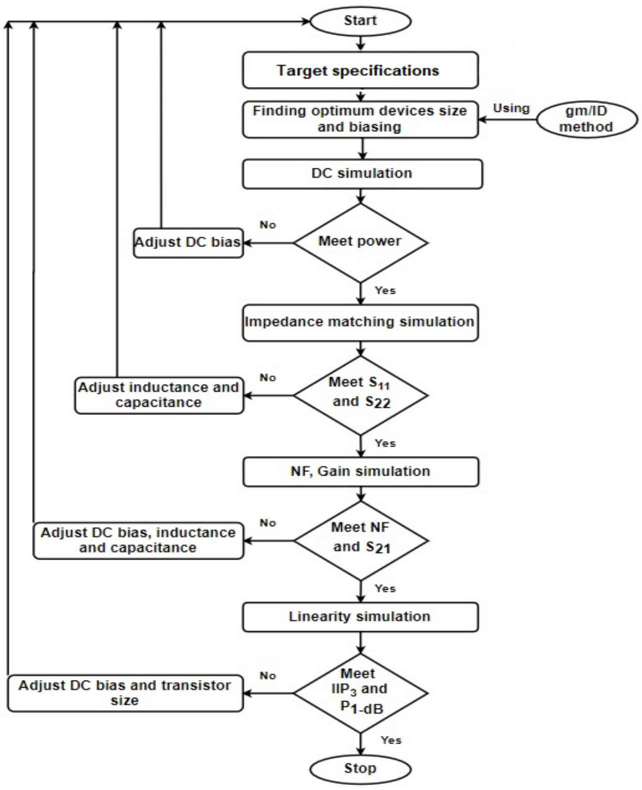

Figure 1. Proposed design methodology flowchart.

2.1 Target Specifications

As the first order of business, when designing an LNA, it seems appropriate to know the target specifications. This is done in terms of several various parameters, like noise, gain, linearity, input and output reflection coefficients. These parameters differ from one application to another. The demonstrated LNA is targeting Wi-Fi, Bluetooth and Zigbee applications. The target design specifications for each application are summarized in Table 1 below based on [4], [10]-[14].

Table 1. LNA design specifications.

Performance parameters	**Bluetooth @ IEEE 802.15.1**	**Wi-Fi @ IEEE 802.11 b**
Noise Figure (NF)	< 3.5 dB	< 3.5 dB
Power Gain (S_{21})	> 15 dB	> 15 dB
1dB Compression Point	> -20 dBm	> -20 dBm
IIP_3	> -15 dBm	> -15 dBm
Input Reflection Coefficient (S_{11})	< -10 dB	< -10 dB
Output Reflection Coefficient (S_{22})	< -10 dB	< -10 dB
Reverse Isolation Coefficient (S_{12})	< -40 dB	< -40 dB
Power	< 10 mw	< 10 mw

2.2 Topology Selection

The second step is to choose the topology that best suits the design specifications for the targeted applications. The IDCCS topology has been chosen for several reasons that will be discussed in detail in this section.

2.2.1 Inductively Degenerated Cascoded Common Source (IDCCS) LNA

As a starting point, a simple CS LNA is selected, as shown in Figure 2. The input impedance is dominated by the gate-source capacitance (C_{gs}). So, it is hard to achieve a pure real impedance without an input impedance matching network.

One of the input impedance matching networks that may be used is a parallel resistor at the input to match with the source resistor, but this is not an optimal solution. Although it may provide the real part of impedance, the imaginary part still exists due to CMOS parasitic capacitance. Also, it adds thermal noise that increases the overall LNA NF.

One of the best solutions to achieve real impedance matching without using a resistor and improve the LNA NF is IDCS topology [4], [15]. IDCS topology uses gate and source inductor to match input impedance, as shown in Figure 3. Gate inductor (L_g) dominates the input capacitance of CMOS (C_{gs}) by forming a series LC circuit at the desired frequency; source inductor (L_s), input transistor transconductance (g_m) and C_{gs} of IDCS produce a real impedance to match the source impedance without using a resistor.

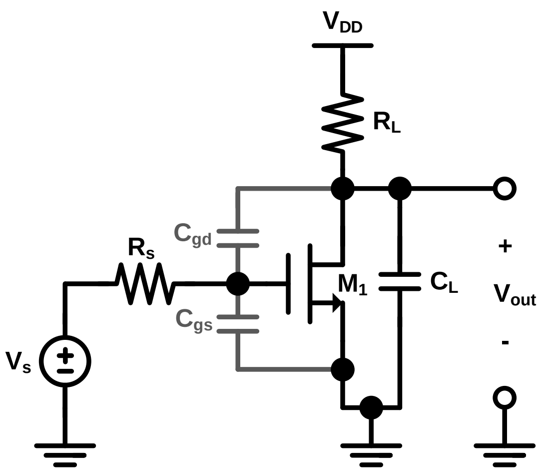

Figure 2. Simple common source CMOS LNA.

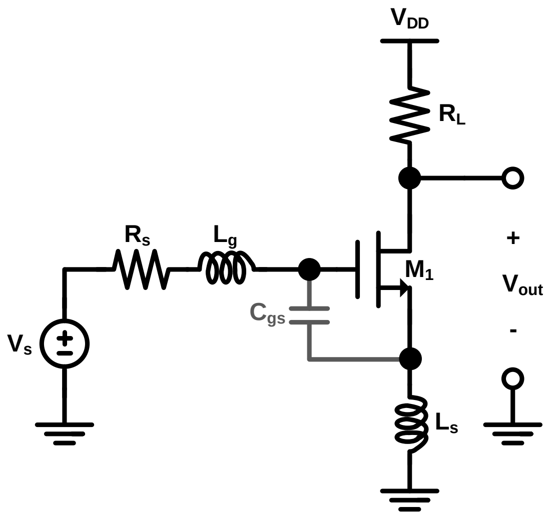

Figure 3. IDCS LNA topology.

2.2.2 Inductively Degenerated Cascoded Common Source (IDCCS) LNA

A small-signal equivalent circuit of the input stage of IDCS CMOS LNA is shown in Figure 4, where the input impedance is Z_{in}.

Applying KVL in the input loop of the circuit in Figure 4, Z_{in} can be found by the following Equations:

$$V_{in} = I_{in} * SL_g + \frac{I_{in}}{SC_{gs}} + (g_m * V_{gs} + I_{in})SL_s \tag{1}$$

where:

$$V_{gs} = \frac{I_{in}}{SC_{gs}} \tag{2}$$

By substituting Equation (2) into Equation (1), we have:

$$V_{in} = I_{in} * SL_g + \frac{I_{in}}{SC_{gs}} + (g_m * \frac{I_{in}}{SC_{gs}} + I_{in})SL_s \tag{3}$$

Then, the input impedance can be found as:

$$Z_{in} = \frac{V_n}{I_{in}} = S(L_s + L_g) + \frac{1}{SC_{gs}} + \frac{g_m * L_s}{C_{gs}} \tag{4}$$

By replacing $s = j\omega$, we have:

$$Z_{in} = \frac{V_n}{I_{in}} = j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \frac{g_m * L_s}{C_{gs}} \tag{5}$$

The real and imaginary parts of the input impedance are shown in Equation (6) and Equation (7), respectively:

$$Re(Z_{in}) = \frac{g_m * L_s}{C_{gs}} \tag{6}$$

$$Im(Z_{in}) = j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} \tag{7}$$

The input impedance of IDCS LNA is similar to the series RLC circuit shown in Figure 5, where the first term and second term shown in Equation (5) are inductive and capacitive, respectively, while the third term is a resistive impedance.

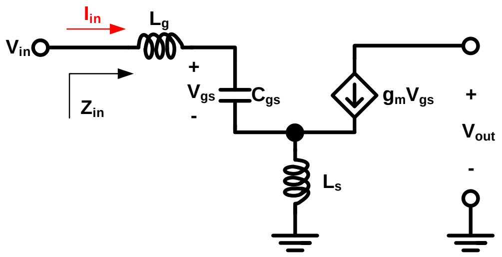

Figure 4. Small-signal equivalent circuit of the input stage of IDCS LNA.

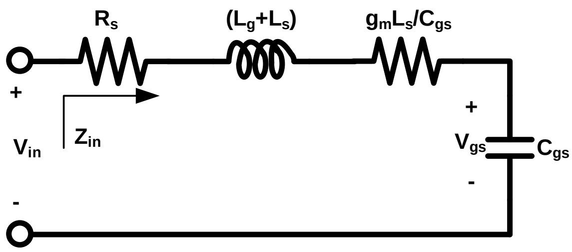

Figure 5. Input equivalent circuit of IDCS LNA.

So, IDCS LNA achieves a resistive input impedance without using a resistor. Generating a resistive impedance using a degenerative source inductor does not generate as much noise as a real resistor; it helps minimize the LNA NF.

To match the input impedance with the source impedance (Z_o) that is usually equal to 50Ω, the real part of Z_{in}, Re(Z_{in}) should be equal to 50 Ω. It depends on transconductance, source inductance and C_{gs}. Also, the imaginary part of Z_{in}, Im(Z_{in}), should be equal to zero, which occurs only at a particular frequency. This frequency is called the resonance frequency $\omega_\circ$, where $\omega_\circ$ is expressed as in Equation (8) [16].

$$\omega_\circ = \frac{1}{\sqrt{(L_s+L_g)(C_{gs})}} \tag{8}$$

At other frequencies, we can't get pure resistive matching. It is worthy to note that the desired matching impedance can be achieved at a particular frequency. Thus, the IDCS topology is proposed for NB LNA.

2.2.3 IDCS Output Impedance Analysis

Generally, in the NB topology, LNA has an inductive load instead of a resistive load, as shown in Figure 6. There are several reasons to use an inductor instead of a resistor on the load. The first one is to minimize the NF, noting that the resistor will add thermal noise. The second one is to maximize the voltage swing, because in DC behaviour, the frequency is zero and the inductor will act as a short circuit which maximizes the voltage swing, while in the resistor case, the voltage swing will be decreased by the amount of DC voltage drop across the resistor. The third one is that, in AC behaviour, the LNA will act as a Low Pass Filter (LPF) in the resistor case, while in the inductor case, it will act like a Band Pass Filter (BPF) at certain frequencies.

To explain how the IDCS LNA with load inductor (L_d) acts as a BPF, we should mention that L_d has a parasitic resistance modelled as a small series resistor (R_{ds}), as shown in Figure 7. a, where the value of R_{ds} depends on the inductor value and its quality factor. For further discussion, the quality factor (Q) must be introduced.

Q is the parameter used to discover the characteristics and performance of the circuit. The most basic definition is embodied in Equation (9) [17]-[18].

$$Q = \omega \times \frac{\text{Energy Stored}}{\text{Average Power Dissipated}}, \text{ where } \omega \text{ is the angular frequency.} \tag{9}$$

Also, Q can be used as a measure of how lossy the component is, as shown in the Equations below:

$$Q_L = \frac{X_L}{R} = \frac{\omega * L}{R} \tag{10}$$

$$Q_c = \frac{|X_c|}{R} = \frac{1}{\omega C R} \tag{11}$$

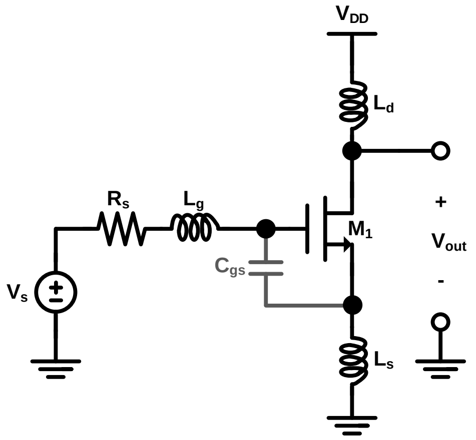

Figure 6. IDCS LNA with load inductor.

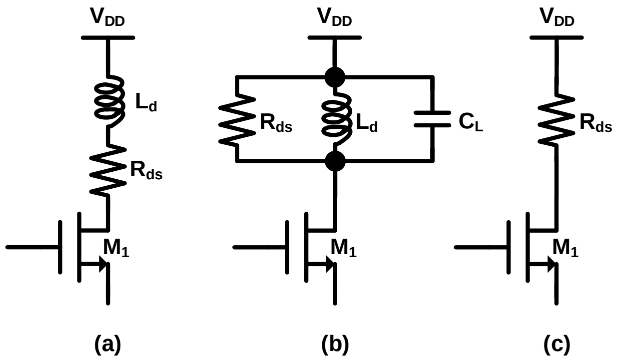

Figure 7. LNA with load inductor (L_d). a) L_d with its series resistor (R_{ds}). b) L_d as a part of parallel RLC circuit. c)LNA load at the resonance frequency (ω_o).

From Equation (10), The value of R_{ds} can be found as expressed in Equation (12).

$$R_{ds} = \frac{L_d * \omega}{Q_{Ld}} \tag{12}$$

where R_{ds} is a series resistor, as shown in Figure 7. (a), L_d is the drain inductor and Q_{Ld} is the quality factor of the inductor L_d.

As shown in Figure 7(a), we have a series (RL) circuit on the load, where the series (RL) circuit can be converted into a parallel (RL) circuit using Equation (13) that shows the quality factor for a parallel (RL) circuit.

$$Q_{Ld} = \frac{R_{dp}}{L_d * \omega} \text{ , then } R_{dp} = Q_{Ld} * \omega * L_d \tag{13}$$

where R_{dp} is the parallel resistor, as shown in Figure 7 (b).

The value of R_{dp} depends on the L_d value and its quality factor and angular frequency. After the conversion, we have a parallel RLC circuit in the load, as shown in Figure 7 (b), L_d and R_{dp} have formed a parallel tuned circuit with C_L, where C_L represents the LNA parasitic capacitance and the input capacitance for the next circuit after the LNA, which might be a mixer or a buffer circuit.

To match the output impedance to 50 Ω, R_{dp} should be equal to 50 Ω and L_d should resonate with C_L at the operating frequency (output resonance frequency), which can be expressed as shown in Equation (14):

$$\omega_o = \frac{1}{\sqrt{L_d C_L}} \tag{14}$$

2.2.4 Cascode IDCS

IDCS topology has bad isolation between input and output due to the Miller capacitor. To solve this problem, cascode IDCS LNA, as shown in Figure 8, has been used to improve the reverse isolation between input and output by reducing the effect of the Miller capacitor, which may cause instability. Transistor M_2 has a minor influence on the noise behaviour of the LNA and its contribution to the total noise can be disregarded [19], because the source of the cascode transistor is connected to a large resistance (M_1 output resistance).

The cascode IDCS has been selected for the designed LNA, since it can achieve narrow-band matching at the input and output at the operating frequency. Also, it can achieve a high gain, minimum noise and high reverse isolation.

2.3 Selecting Device Size and Biasing Voltages

The next step is to find the optimum device size and biasing voltages to obtain the minimum NF and maximum gain by considering the power specification for the demonstrated LNA. The g_m/I_D method is used to find the optimum device size and biasing voltages, because there's a disconnection between the actual transistor behavior and the simple square-law model [20]. Any square law-driven design optimization will be far from the simulation results.

The solution to solve this problem is to begin the design with precomputed simulation data using hand calculations. To achieve our goal in maintaining a systematic design methodology in the absence of a set of functional compact MOS equations, a strategy of using lookup tables or charts is followed. These tables or charts are obtained from the technology characterization via DC Sweep simulation of the transistor model, as shown in Figure 9.

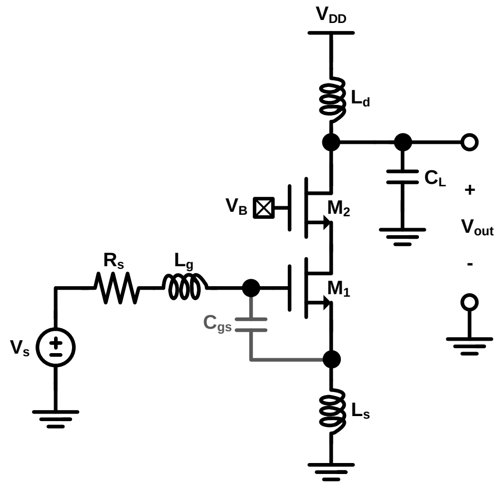

Figure 8. Cascode IDCS LNA.

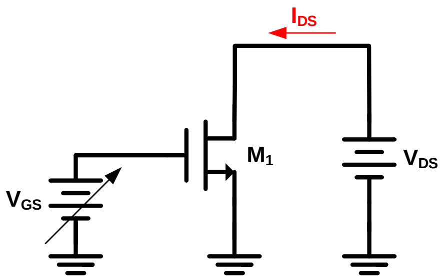

Figure 9. CMOS test circuit for acquiring g_m/I_D charts.

To find the optimum device size and biasing voltages for minimum NF and maximum gain from the resulting charts, we should discuss Equation (15) that expresses the noise factor in general [2], [10], [21].

$$F = F_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2 \tag{15}$$

where F_{min} is the minimum noise factor as expressed in Equation (16), R_n is the noise resistance, G_s is the source conductance, Y_s and Y_{opt} are the source admittance and the optimum admittance, respectively.

$$F_{min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_t}\sqrt{\gamma\delta(1-|c|^2)} \tag{16}$$

To achieve minimum NF, we should satisfy the two parts of Equation (15). First, we should achieve minimum noise from the core transistor by finding the optimum value for biasing voltages and sizing. Second, F_{min} can be achieved by the input matching circuit by making the source admittance (Y_s) equal to the optimum source admittance (Y_{opt}). To obtain minimum NF from the core transistor, we should increase the value of cut-off frequency (f_t). From the first resulting chart between f_t and g_m/I_D shown in Figure 10, we see that as long as g_m/I_D is low, f_t will be high and NF is low, but as long as g_m/I_D is high, the gain will be high as well. There is always a trade-off between NF and gain, noting that we need optimum values for both of them.

The y-axis in Figure 10, shows the cut-off frequency (f_t=g_m/Cgs) and the x-axis shows the gm-over-ID value (g_m/I_D).

Any increase in the V_{od} value will cause an increase in f_t and a decrease in the NF value, since $V_{od}=2/(g_m/I_D)$, but at the same time, it will cause the power to be increased and the gain to be decreased.

By multiplying f_t with g_m/I_D, the resulting peak value will be the best point to choose the optimum value of V_{od} for maximum gain and minimum noise without increasing the power, as shown in Figure 11, where the y-axis shows the multiplication between cut-off frequency and g_m/I_D (FOM=ft*gm_over_ID) and the x-axis shows the overdrive voltage (V_{OD}).

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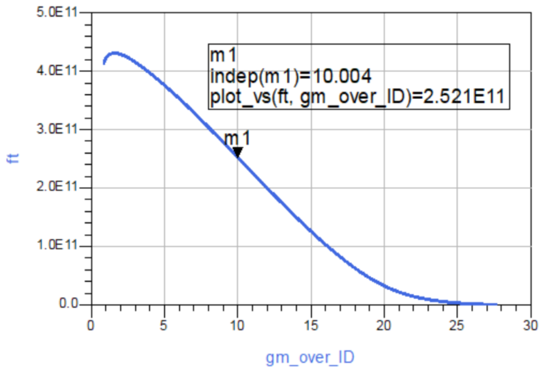

Figure 10. f_t *versus* g_m/I_D for an nMOS transistor.

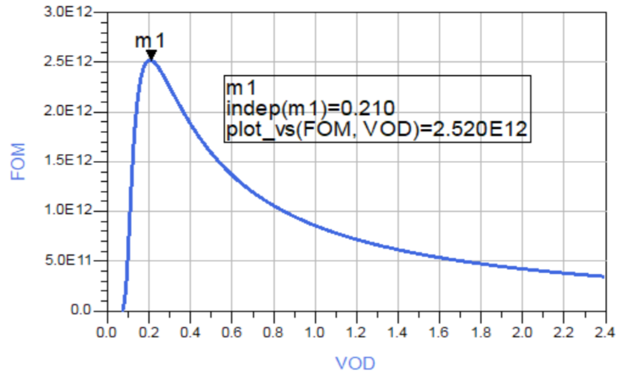

Figure 11. (f_t g_m/I_D) *versus* V_{od} for an nMOS transistor.

From the value of V_{od}, the optimum value of g_m/I_D can be found, where $g_m/I_D = 2/V_{od}$. After finding the optimum value of g_m/I_D, the optimum values of V_{gs} and current density (I_D/W) can be found in Figures 12 and 13, respectively. Figure 13 shows that the optimum values for g_m/I_D, V_{gs} and I_D/W are 10, 0.65 V and 29.73, respectively.

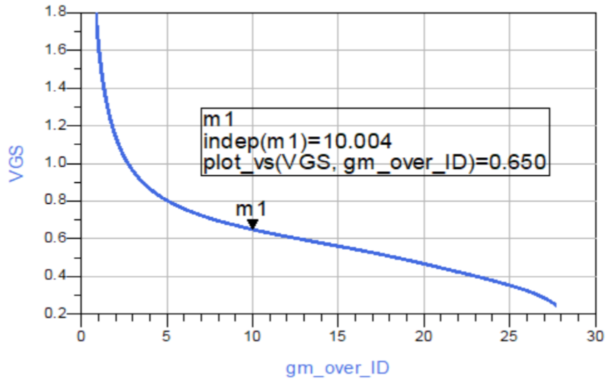

Figure 12. V_{gs} versus gm/I_D for an nMOS transistor.

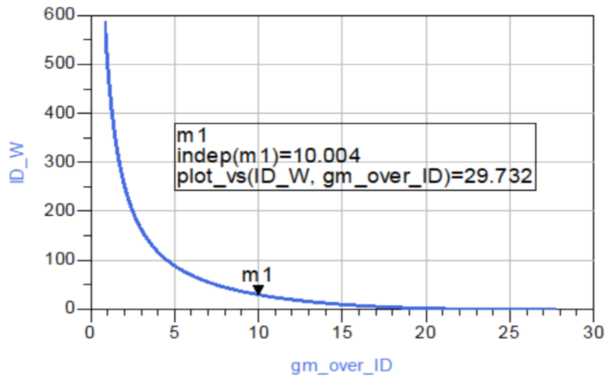

Figure 13. (I_D/W) versus g_m/I_D for an nMOS transistor.

The value of I_D has been selected based on the power budget for each standard. For example, for Wi-Fi and Bluetooth standards (when operated at 2.4 GHz), the maximum power is 10 mW, where power $=I_D*V_{DD}$. In the design circuit, the value of V_{DD} that has been used is 1.8V and the maximum value of I_D is 5.5 mA. After finding the I_D value, from the optimum I_D/W value that was found previously, we can now obtain the optimum device size for each standard for minimum NF, maximum gain and specific power.

2.4 Selecting RF Inductor

The values of RF inductors (Lg, Ls and Ld) should be chosen carefully based on several factors:

1) Inductor value at the operating frequency (2.4 GHz).
2) Inductor quality factor at the operating frequency, as it affects NF and power gain.
3) Inductor self-resonance frequency (SRF). It should be far from the operating frequency, because at SRF, the inductor resonates with its parasitic capacitance [16]. Figure 14 shows how the inductor acts at its SRF while the input impedance is at its peak and the effective inductance is zero, since the negative capacitance reactance (X_C=1/jωc) cancels the inductive reactance (X_L = jωL).

All the TSMC 0.18-µm PDK inductors were being tested at the operating frequency and the results are summarized in Table 2. To choose the best inductor with the highest quality factor, the SRF should be far away from the operating frequency, w is the inductor width, rad is the inductor radius, nr is the number of turns and Q is the inductor quality factor.

Figures 15 and 16 show the tested inductor value and its quality factor at the operating frequency.

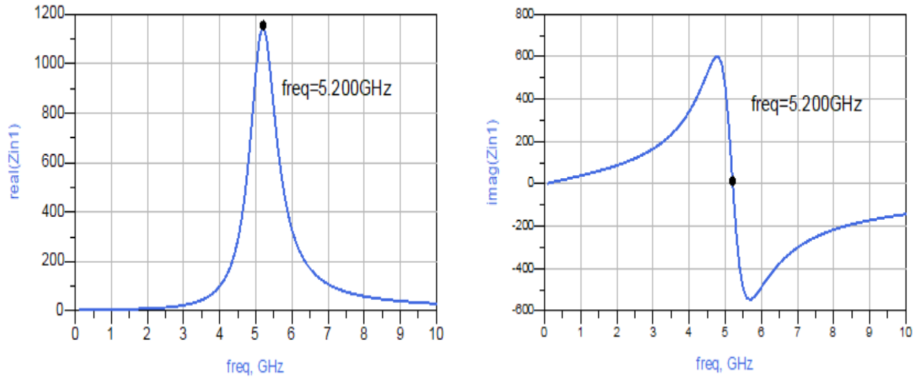

Figure 14. Representing how the inductor acts at its self-resonance frequency (SRF).

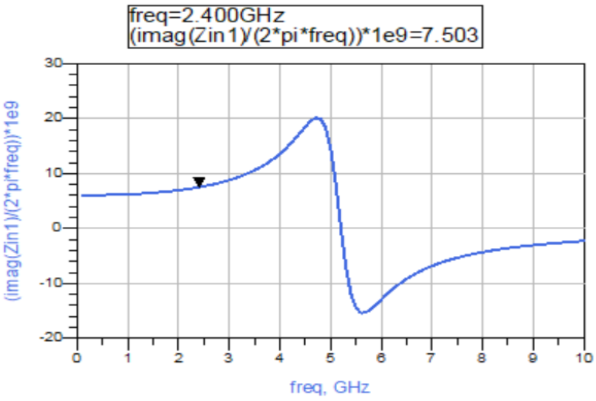

Figure 15. Representing the tested inductor value at the operating frequency.

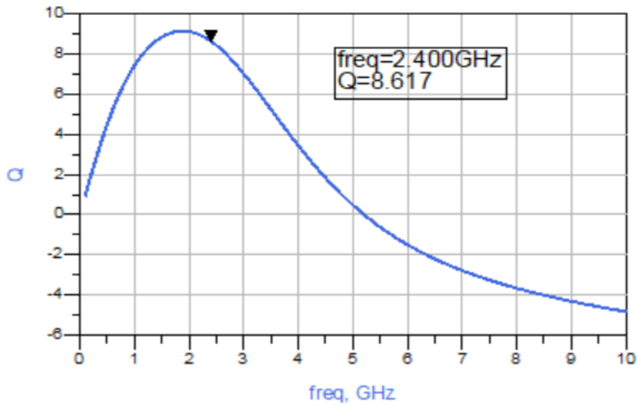

Figure 16. Representing the tested inductor quality factor at the operating frequency.

Table 2. TSMC 0.18-μm PDK inductors.

L1	**L (nH)**	**W (μm)**	**rad (μm)**	**nr**	**Q**	**SRF (GHz)**
Minimum inductance @ 2.4 GHz	0.22	15	30	0.5	7	0.1
Maximum inductance @ 2.4 GHz	25.6	15	125	5.5	5.3	3
Med. @ 2.4 GHz	9.9	15	64	5.5	1.4	5.5
L2	**L (nH)**	**W (μm)**	**rad (μm)**	**nr**	**Q**	**SRF (GHz)**
Minimum inductance @ 2.4 GHz	0.48	30	30	1.5	7.86	0.1
Maximum inductance @ 2.4 GHz	14.64	30	70.3	5.5	1.15	3
Med. @ 2.4 GHz	9.6	30	37	5.5	2.9	4.5
L3	**L (nH)**	**W (μm)**	**rad (μm)**	**nr**	**Q**	**SRF (GHz)**
Minimum inductance @ 2.4 GHz	0.23	15	40	1	9.3	0.1
Maximum inductance @ 2.4 GHz	26.6	15	120	5	4.16	3
Med. @ 2.4 GHz	9.5	15	76	5	7.6	5.5
L4	**L (nH)**	**W (μm)**	**rad (μm)**	**nr**	**Q**	**SRF (GHz)**
Minimum inductance @ 2.4 GHz	0.54	30	65	1.5	7.24	0.1
Maximum inductance @ 2.4 GHz	28.54	30	117	5	0.74	2.5
Med. @ 2.4 GHz	9.26	30	65	4.9	5.34	4

3. Simulation Result

The demonstrated LNA has been designed using the TSMC CMOS 0.18 μm technology and simulated using ADS RF circuit simulator. Figure 17 shows the design circuity schematic for Wi-Fi and Bluetooth standards with all on-chip components.

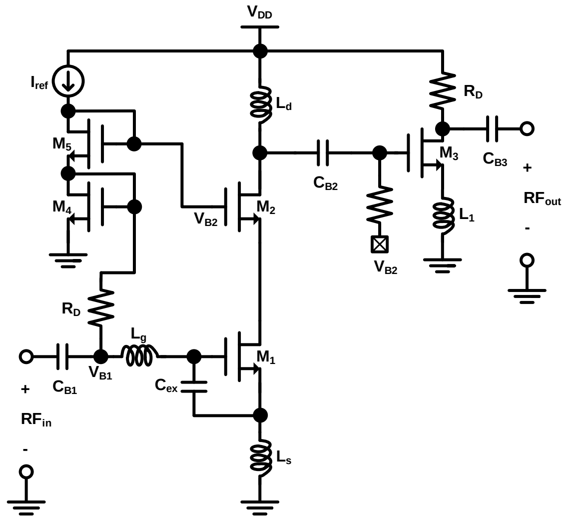

Figure 17. The designed IDCS LNA schematic targeted for Wi-Fi and Bluetooth standards.

The designed LNA uses the source-degenerative cascode topology. The input stage is composed of L_s, L_g, M_1 and C_{ex}. External capacitor (C_{ex}) has been added between gate and source of the input transistor M_1 to minimize design area and NF at low power consumption [19], [21].

These inductors and external capacitors are used for input matching. Transistors M_4 and M_5 are used as LNA biasing circuits, forming a current mirror to set bias current with R_B. The output matching network consists of M_2 and L_D. The drain inductor L_D should resonate with the total drain capacitance and provide a high enough impedance to obtain a decent gain, hence achieving the desired frequency.

The last stage in the design of the design circuity is the output buffer. This buffer is incorporated into the overall LNA design to match the output impedance to a network analyzer for measurement purposes. The common source buffer translates the high impedance path at the gate of M_3 to the low impedance path at the drain of M_3. In addition, coupling capacitances C_{B1}, C_{B2} and C_{B3} are at the input and output of the cascode stage and the buffer stage, respectively. All design values of the components and biasing voltages are summarized in Tables 3 and 4.

Table 3. The designed IDCS LNA component values.

Component	Value
Transistor M_1 width, W_1	163.5 µm
Transistor M_2 width, W_2	96 µm
Transistor M_3 width, W_3	160 µm
Transistor M_4 width, W_4	9 µm
Transistor M_5 width, W_5	22.5 µm
Transistors' length, L	0.18 µm
L_g	9.42 nH
L_s	1.25 nH
L_D	9.42 nH
L_1	2.2 nH
C_{ex}	188 fF
C_{B1}, C_{B2} and C_{B3}	5 pF
R_{B1}, R_{B2}	50 kΩ
R_D	50 Ω
V_{dd}	1.8 V
I_{ref}	200 µA

Table 4. The designed IDCS LNA biasing voltages.

Transistor	Biasing voltages
M_1	V_D =548 mV, V_G=629 mV, V_S=4.14 mV
M_2	V_D =1.8 V, V_G=1.34 V, V_S=548 mV
M_3	V_D =1.56 V, V_G=629 mV, V_S=8.4 mV
M_4	V_D =629 mV, V_G=629 mV, V_S=0 mV
M_5	V_D =1.34 mV, V_G=1.34 V, V_S=629 mV

Figure 18 shows the achieved simulation results for power gain (S_{21}) and maximum power gain. The demonstrated LNA has achieved more than 22 dB S_{21} at the desired frequency (2.4 GHz) and is very close to the maximum gain value that can be achieved at the desired frequency. As shown in Figure 19, the design circuity achieved an NF of 1.75 dB, almost equal to the minimum NF that can be achieved at the desired frequency. Figure 20 shows the achieved reverse transmission coefficient (S_{12}), input reflection coefficient (S_{11}) and output reflection coefficient (S_{22}) at 2.4 GHz. The stability simulation result is shown in Figure 21, where the stability coefficient is greater than one, which means that the designed LNA is unconditionally stable at the desired frequency.

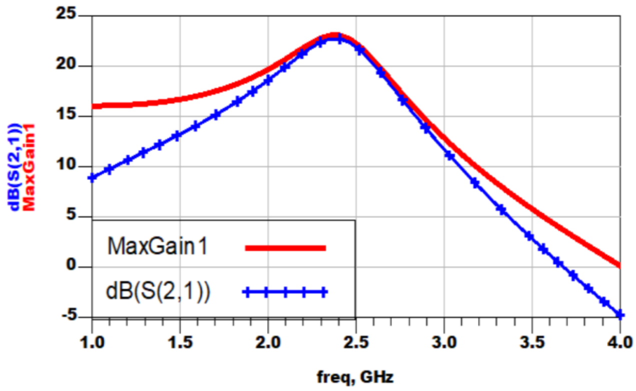

Figure 18. Maximum gain and S_{21} simulation results of IDCS (Wi-Fi and Bluetooth) LNA.

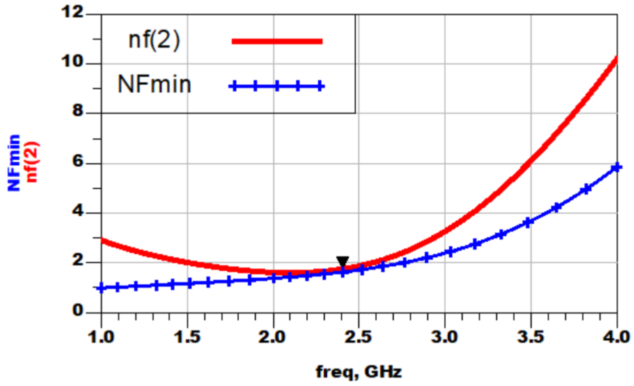

Figure 19. NF and minimum NF simulation results of IDCS (Wi-Fi and Bluetooth) LNA.

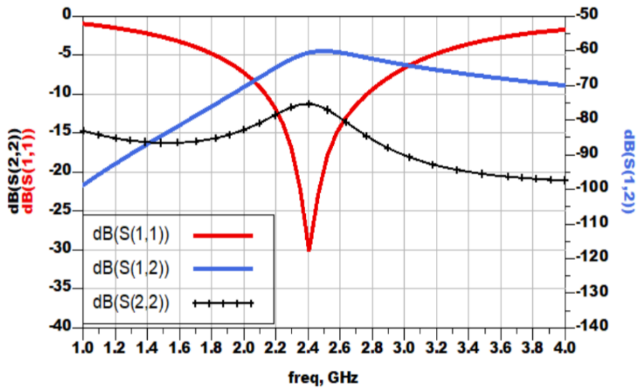

Figure 20. S_{11}, S_{22} and S_{12} simulation results of IDCS (Wi-Fi and Bluetooth) LNA.

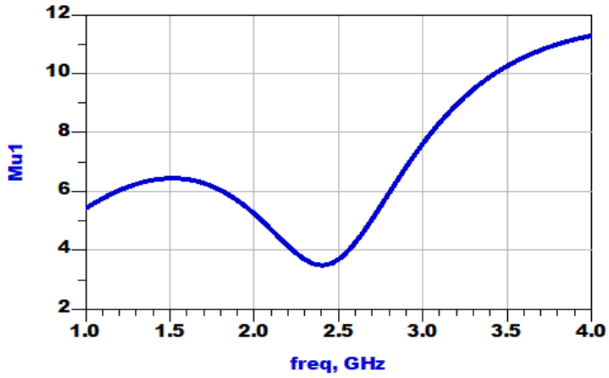

Figure 21. Stability factor simulation result of IDCS (Wi-Fi and Bluetooth) LNA.

Simulation results of $P_{1\text{-dB}}$ compression point and IIP_3 as shown in Figure 22 and Figure 23, are –19 dBm and – 13.5 dBm, respectively. All targeted and achieved performance parameters of (Wi-Fi and Bluetooth) IDCS LNA are summarized in Table 5.

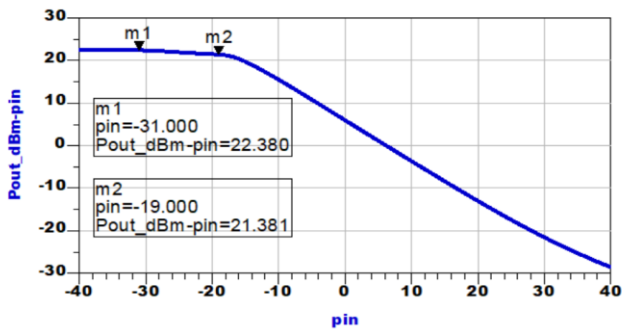

Figure 22. Output power gain *versus* input power p_{in} of IDCS (Wi-Fi and Bluetooth) LNA.

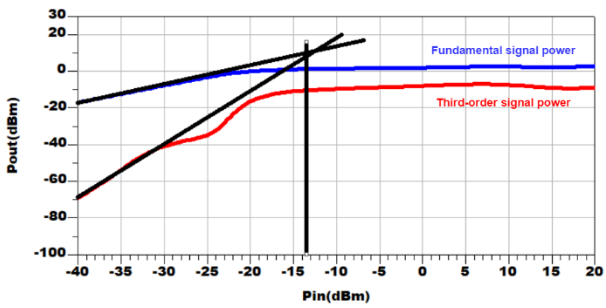

Figure 23. IIP_3 simulation result of IDCS (Wi-Fi and Bluetooth) LNA.

The demonstrated LNA performance has been simulated for different process corners, supply voltages and temperatures at 2.4 GHz. The Figures below (Figure 24–Figure 28) show the corners' simulation

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(Typical-Typical corner (TT), Fast-Fast corner (FF) and Slow-Slow corner (SS)) results of LNA performance parameters when the LNA operates for Wi-Fi and Bluetooth standards over temperature and voltage variations. As shown from the figures below, the designed LNA has a good performance over process, voltage and temperature (PVT) variations.

Table 5. All targeted and achieved performance parameters of (Wi-Fi and Bluetooth) IDCS LNA.

Performance parameters	Targeted specifications	Achieved results
NF	< 3.5 dB	1.75 dB
S_{21}	> 15 dB	22.75 dB
S_{11}	< -10 dB	-30.11 dB
S_{22}	< -10 dB	-11.23 dB
S_{12}	< -40 dB	-60.49 dB
IIP_3	> -15 dBm	-13.5 dBm
$P_{1\text{-}dB}$	> -20 dBm	-19 dBm
Power consumption	< 10 mw	6.16 mW

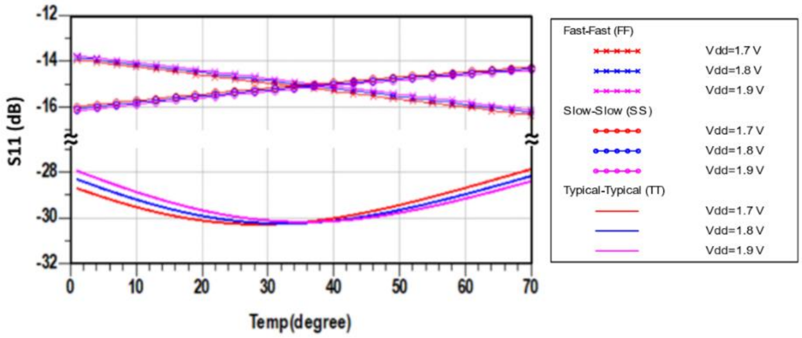

Figure 24. S_{11} simulation results over temperature and voltage variations of the demonstrated LNA at TT, FF and SS corners.

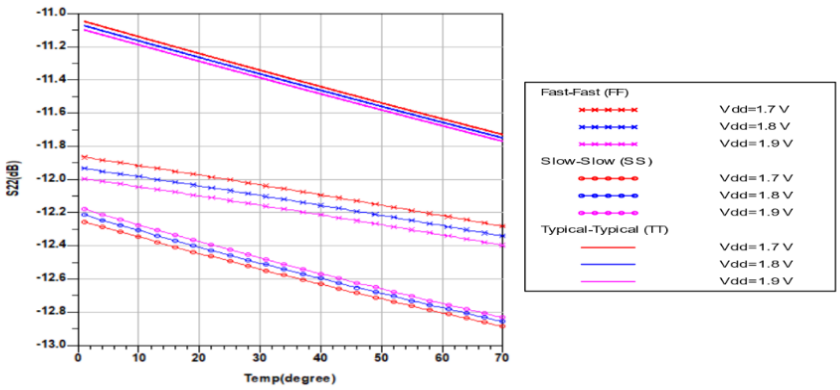

Figure 25. S_{22} simulation results over temperature and voltage variations of the demonstrated LNA at TT, FF and SS corners.

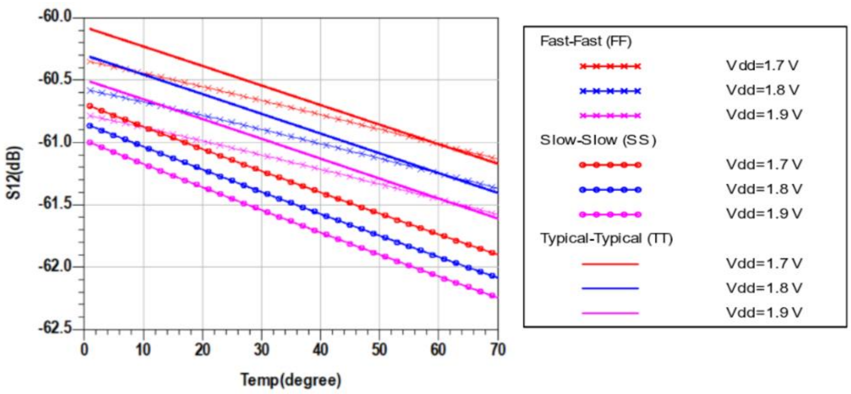

Figure 26. S_{12} simulation results over temperature and voltage variations of the demonstrated LNA at TT, FF and SS corners.

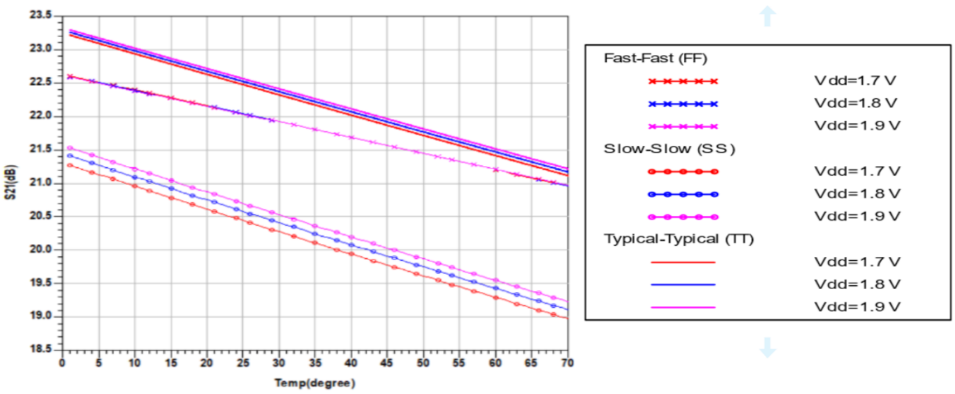

Figure 27. S_{21} simulation results over temperature and voltage variations of the demonstrated LNA at TT, FF and SS corners.

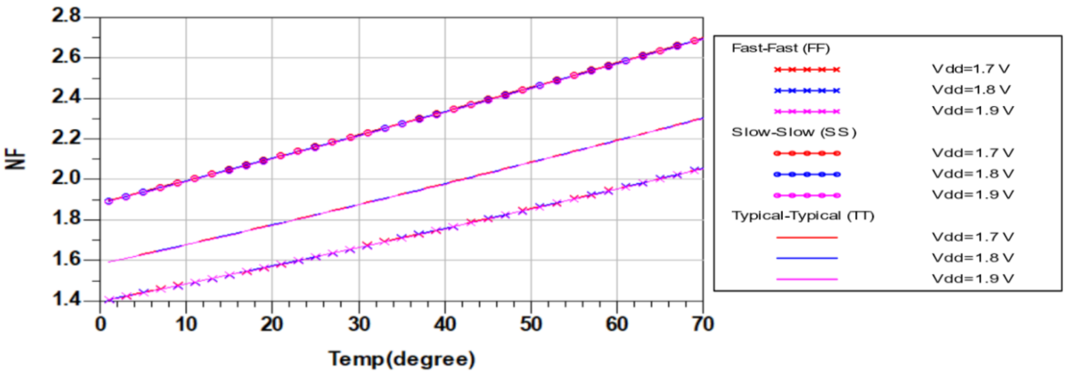

Figure 28. NF simulation results over temperature and voltage variations of the demonstrated LNA at TT, FF and SS corners.

Table 6 shows a comparison of state-of-the-art LNA performances. Because the LNA performance depends on several parameters, like NF, gain, linearity and power consumption, the Figure of Merit (FOM) equation has been used to compare the demonstrated LNA performance with other LNA circuit performances. The FOM equation includes Gain, NF, IIP_3, operation frequency (f_o) and power consumption (P_{DC}) as follows [22]-[23]:

$$\mathrm{FOM[GHz]} = \frac{\mathrm{Gain[Lin.]} * \mathrm{IIP_3[mW]} * \mathrm{f_o[GHz]}}{(\mathrm{F}-1) * \mathrm{P_{DC}[mW]}} \tag{17}$$

The demonstrated LNA has the best FOM among the published NB CMOC LNAs shown in Table 6.

Table 6. A comparison of state-of-the-art LNA performances.

Ref.	[This work]	[4] 2015	[5] 2018	[6] 2020	[7] 2016	[8] 2017	[9] 2017
f_o [GHz]	2.4	2.4	2.4	2.4	2.4	2.4	2.4
Tech. [nm]	180	180	180	180	90	180	130
Integration	Fully	Partially	Partially	Fully	Fully	Fully	Fully
Type of results	Simulation	Simulation	Simulation	Measurement	Measurement	Simulation	Simulation
P_{DC} [mW]	6.16	9.68	48	2	3	NA	NA
NF [dB]	1.75	1.2	2.62	8.7	1.8	3.14	10.2
S_{21} [dB]	22.75	14.55	18.24	14.1	13	12.68	10.97
S_{11} [dB]	−30.11	−14.15	−15.95	−14	−10	−13.5	−5.56
S_{22} [dB]	−11.23	−10.6	−13.89	NA	−10	−10	NA
S_{12} [dB]	−60.49	−19.46	−46.05	NA	−20	−33.85	NA
IIP_3 [dBm]	−13.5	−22.41	NA	NA	−8.9	NA	17
$P_{1\text{-}dB}$ [dBm]	−19	−16.43	NA	−14.6	NA	NA	NA
FOM [GHz]	8.07	0.12	NA	NA	3.75	NA	NA

4. CONCLUSIONS

This paper presented a simple and comprehensive design methodology for narrow-band CMOS LNA. The methodology is applied in realizing the IDCCS LNA for Wi-Fi and Bluetooth standards. The g_m/I_D method had been used to optimize the device values for both maximum power gain and minimum NF without exceeding the specified power budget. The circuit is implemented with TSMC CMOS 0.18µm technology using Advance Design System (ADS) RF simulation toolkit. Following the proposed methodology, the design has achieved a power gain (S_{21}) of 22.75 dB, a reverse isolation (S_{12}) of -60.49 dB, input and output reflection coefficients (S_{11} and S_{22}) of -30.11 dB and -11.23 dB, respectively. An NF of 1.75 dB has been achieved with the linearity metrics ($P_{1\text{-}dB}$ and IIP_3) of (-19 dBm and -13.5 dBm).

Note that with a stability factor of 3.48, the circuit is unconditionally stable at the operating frequency of 2.4 GHz. The design power consumption is 6.16 mW from a voltage supply of 1.8V. A superior FOM of 8.07 was obtained using this design methodology. With PVT variations, the design performance metrics still fall within the design specifications with minimal deviations from the typical values obtained. Future work will include an integrated circuit fabrication of the used LNA.

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ملخص البحث:

تعرض هذه الورقة طريقةً لتصميم مكبّر متكامل ضيّق النّطاق منخفض الضّجيج. ولبيان فاعلية الطريقة المقترحة، تمّ تصميم مكبّر منخفض الضّجيج وفق معايير (واي فاي) و (بلوتوث) عند ترددٍ مقداره 2.4 جيجاهيرتز، وقد تمّ تنفيذ دارات التّصميم باستخدام تكنولوجيا سي موس 0.18 ميكروميتر؛ ومع ذلك، فإنّ الطريقة المقترحة يمكن تطبيقها بشكلٍ مكافيء على أي عُقدة عمليات أخرى. وبهذه الطريقة، يمكن الحصول على الحجم الأمثل والانحيازات المثلى للترانزستورات المستخدمة دون خرْق لميزانية القُدرة.

كذلك، تحدد الطريقة المقترحة معايير اختيار ملفات التّرددات الراديوية المستخدمة على الرقاقة بناءً على معامل الجودة، وتردد الرنين الذاتي، والمساحة. ويحقق التّصميم المقترح كسب قُدرة مقداره 22.75 ديسيبل، بينما يبلغ فقْد الرجوع للمدخل 30.11 ديسيبل، والعزل العكسي -60.49 ديسيبل، وفقد الرجوع للمخرج -11.23 ديسيبل. كما تبلغ المتغيرات الخطية لكلٍ من نقطة الانضغاط P1-dB و IIP3: (-19dBm) و (-13.5dBm)، على الترتيب. أما فيما يتعلق برقم الضّجيج فقد بلغ 1.75 ديسيبل، بينما يستهلك المكبّر قُدرة مقدارها 6.16 ميلي واط من مصدرٍ للقُدرة يعطي فرقاً في الجهد يبلغ 1.8 فولت.