Jordanian Journal of Computers and Information Technology (JJCIT), Vol. 08, No. 02, June 2022.

FULLY OPTIMIZED ULTRA WIDEBAND RF RECEIVER FRONT END

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(Received: 6-Feb.-2022, Revised: 22-Mar.-2022, Accepted: 13-Apr.-2022)

ABSTRACT

This paper proposes a novel and fully optimized ultra-wideband RF receiver front end in UMC 180nm 1P6M CMOS process. The heterodyne architecture used in this work does not use the on-chip image reject mixer. The proposed receiver consists of a cascode inductively degenerated common source differential low noise amplifier and a folded Gilbert down-conversion mixer. The differential low-noise amplifier eliminates the use of active balun and improves the noise performance, while the folded architecture reduces the power dissipation of the receiver. The post-layout simulated result shows that the receiver has a voltage gain of 15.2 - 19.8dB, a noise figure of 4.8 - 8.9dB, a third-order input intercept point (IIP3) of -6.3 to -2.9dBm and consumes 31.5mW from a 1.8V supply. The receiver has a good reverse isolation S12 of -42 to -59dB due to cascode configuration and occupies an area of 2.55mm^2.

KEYWORDS

CMOS, UWB, Noise figure, IIP3, Receiver front end.

1. INTRODUCTION

Federal Communications Commission (FCC) has allocated a large frequency range of 3.1 to 10.6GHz (spectrum of 7.5GHz) for high-speed and short-distance communication. This ultra-wideband (UWB) IEEE 802.15.3a standard is used for wireless personal area network that transmits an extremely low signal power over a short distance at a high data rate (up to 480Mbps). Due to its ultra-wide bandwidth, people will popularly use it for sharing photos, music, videos, voice and data among laptops, PCs and mobiles connected in a network at home or office. There are two possible techniques to exploit the allocated spectrum. One is the multiband (MB) approach and the other is the Impulse-Radio (IR) approach [1]. In Multiband–UWB (MB-UWB), as specified in IEEE 802.15.3a standard, the entire bandwidth of 7.5GHz is divided into 5 band groups of 14 bands with a spacing of 528MHz, as shown in Figure 1, with OFDM (Orthogonal Frequency Division Multiplexing) modulation and frequency hopping scheme. The other possibility is the so-called Impulse-Radio-UWB (IR-UWB) based on transmission of very short pulses, with position or polarity modulation.

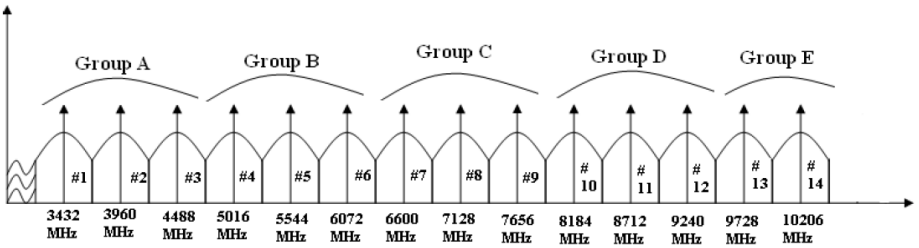

Figure 1. MB-UWB frequency plan.

UWB receiver front ends are challenging to researchers, as they require high receiver gain, high linearity, low signal-to-noise ratio (SNR) and minimum power consumption over a wide bandwidth. UWB is open to reception of undesired narrowband signals from WiFi and WiMAX systems under IEEE 802.11a/b/g as well as other UWB transmitters operating in the same range nearby. Due to narrowband jammers, nonlinearities present in the receiver can cause cross-modulation distortion, which further degrades the signal-to noise ratio. Hence, linearity (both IIP3 and IIP2) specification needs to include the distortion effects.

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So far, several UWB receivers have been reported in literature [2]-[3]. In [2], a UWB direction conversion receiver for 3-5 GHz has been reported. In this research, the authors have achieved a receiver gain of 22dB, an NF of 17dB and a linearity (IIP3) of -6dBm while consuming 16mw from a supply of 2V in 0.18µm CMOS process. Although the receiver front-end has been fully integrated, it does not cover the full bandwidth of UWB from 3.1 to 10.6GHz and has a poor NF. The receiver front-end in [3] has been fabricated in 0.13µm Bi-CMOS process. The Bi-CMOS process has its advantages over the conventional CMOS process, but it is costly and consumes large power. Although the receiver implemented in this work shows a high gain of 52dB and a good IIP3 of -2.7 to -4.5dBm, it consumes a large power amounting to 88mw.

This paper describes designing and simulating of an optimized UWB receiver front end for narrowband and wideband jammers. Section 2 describes the receiver architecture. Specifications for the receiver are given in Section 3. Section 4 covers designing the LNA, mixer and BPF. The simulation results are discussed in Section 5, followed by a conclusion in Section 6.

2. RECEIVER ARCHITECTURE

Typical receiver architectures are direct-conversion receivers and heterodyne receivers. Direct conversion receivers are popular due to their simple architecture, low cost and high integrity. However, they have a problem of DC offset as well as sensitivity to narrowband jammers. Second-order distortion in base band can be another problem of direct-conversion receivers. Due to all these problems, there is a degradation of SNR in such receivers. Heterodyne receivers are less sensitive to second-order distortion and hence to SNR, but can possess various other problems like power consumption and image rejection. Image reject filter or image reject mixer is used for removing the image, but designing such mixer is a challenge. It requires an accurate quadrature local oscillator over a wide fractional bandwidth. In addition, it consumes significant power compared to traditional mixer. After considering the various pros and cons of direct-conversion and heterodyne receiver architectures, a new technique is proposed as an alternative to classical heterodyne receivers. In this proposed receiver architecture shown in Figure 2(a), the problem of image rejection is avoided by selecting an IF of 2.64GHz, so that all images fall below 2.64GHz. Therefore, an additional band pass filter with lower cut-off frequency of around 2.64GHz is used externally at input to remove all images as depicted in the frequency plan for the proposed receiver in Figure 2(b). Although wideband receivers normally use the wideband LO, the solid LO with wide IF has been selected to customize this heterodyne receiver, so that all the images fall below 2.64GHz as explained. Such UWB receivers find application in digital cameras and portable music players which frequently require data transfer of the order of a few gigabytes.

2.1 Design Methodology

The prime objective of this research is the optimization of performance parameters of UWB receiver front end. The performance parameters include receiver gain, noise figure, IIP3 and power dissipation. A comprehensive review of recently published works reveals that most researchers used the direct-conversion receiver due to its simplicity in addition to that it is, easy to design and requires less area due to on-chip components.

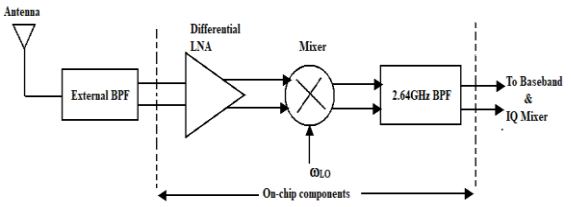

Figure 2(a). Proposed receiver architecture.

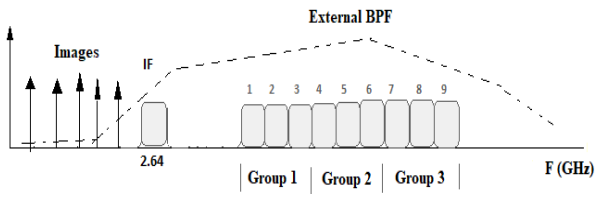

Figure 2(b). Frequency plan for the proposed receiver.

The study also reveals that most authors avoided the use of on-chip inductors as they require more area and have a poor quality factor. The main research gap in these previously published works is that nearly all works were concentrated on reducing area while giving least attention to optimizing performance parameters, which is at most important, particularly at ultra-wide bandwidths. Some

papers have suggested the use of active inductors as an inductorless design to reduce the area. But, active inductors degrade the noise performance of receivers.

This paper tried to fill this research gap of optimizing performance parameters like gain, NF, IIP3 and power dissipation while giving less attention at area. The novelty of this work is that in this paper, a customized heterodyne receiver without image reject filter is designed without compromising on advantages of conventional heterodyne receivers as discussed above. The design methodology used in this work is based on the two well-known Frii's formulae [4]-[5] given by Equation 1 and Equation2 for cascaded blocks.

$$\mathrm{NF} = \mathrm{NF}_1 + \frac{\mathrm{NF}_2 - 1}{\mathrm{G}_1} + \frac{\mathrm{NF}_3 - 1}{\mathrm{G}_1\mathrm{G}_2} + \cdots \quad (1)$$

$$\mathrm{IIP3} = \frac{1}{\frac{1}{\mathrm{IIP3}_1} + \frac{\mathrm{G}_1}{\mathrm{IIP3}_2} + \frac{\mathrm{G}_1\mathrm{G}_2}{\mathrm{IIP3}_3} + \cdots + \frac{\mathrm{G}_1 \ldots \mathrm{G}_n}{\mathrm{IIP3}_n}} \quad (2)$$

Here, Equation 1 is for the overall NF of cascaded stages and Equation 2 is for the overall IIP3 of cascaded stages. From these equations, it is clear that the overall noise figure is dominated by the LNA, whereas the overall IIP3 is dominated by the mixer. Thus, there is a trade-off between noise figure and IIP3 which can be optimized by selecting their respective gain. Since this is an ultra wideband design, further optimization can be achieved by appropriately selecting the topology of LNA and mixer at the circuit level. In this design, differential inductively degenerated common source low-noise amplifier is selected to achieve input matching and low noise and to eliminate active balun. Similarly, a folded Gilbert mixer with load inductors is selected to achieve high IIP3 and low power.

3. RECEIVER SPECIFICATIONS

3.1 Receiver Linearity

As discussed in Section 2, UWB heterodyne receivers are sensitive to narrowband jammers, which in turn degrades the SNR of the receiver. In-band interferers include WiMAX and WiFi devices. In addition to these in-band interferers, a wideband jammer from another transmitting UWB system will produce cross-modulation distortion. UWB transmitter transmits an average power of -10.3dBm. If it is assumed that there is a noise figure of 8dB and an overall gain of 18dB for the LNA and mixer, then to overcome the cross-modulation distortion, the linearity; i.e., IIP3 of the receiver needs to be -8dBm to maintain the link margin of the receiver. Hence, the receiver was designed for an IIP3 of -8dBm.

3.2 Receiver Gain and Noise Figure

It is well known that there is a trade-off between gain and noise figure of the receiver. Generally, it is advantageous to provide a large gain in the receiver front-end, but this will increase the power consumption and degrade the linearity (IIP3). As the receiver consists of LNA and mixer, maximum gain will be provided by the LNA to ease the noise figure requirement on the mixer. Hence, the goal will be to keep front-end gain between 15 dB and 20dB.

4. LNA - MIXER DESIGN AND ANALYSIS

4.1 UWB LNA Design

Selecting the proper topology for the LNA, satisfying the specifications is a challenging task [6]-[7]. There are predominantly three topologies for wideband LNA design. These are: (1) Resistive shunt feedback amplifiers with input and output matching (2) Inductively degenerated common-source amplifier with LC input and output matching (3) Distributed amplifiers. In resistive feedback amplifiers, input matching is achieved by means of resistive termination. This gives a good matching, but the overall noise figure degrades. The power consumption of such circuits is also large. The distributed amplifiers are bulky, consume a large area and are power hungry.

Figure 3 depicts the schematic of the proposed ultra-wideband LNA. The differential configuration is used, which filters out the second-order harmonics and is suitable for a balanced mixer, which is also differential. This reduces the intermediate balun for converting the single ended output of the LNA

into a differential signal for the mixer. LNA uses an inductively degenerated common-source technique widely used in narrow-band designs with multisection reactive network, so that the overall input reactance is resonated over a wider bandwidth. As shown in Fig. (3), inductor Lp1 and capacitor Cp1 provide wide-band matching. Thus, a wideband input matching is achieved along with a good noise performance. To increase the flexibility in achieving perfect match, an inductor (Lg1) is placed in series with the gate of MOS transistor (M1) and a capacitor (Ct1) is also placed between the gate and the source of MOS transistor (M1). Here, the cascode configuration of MOS transistors M1 and M2 provides better reverse isolation (S12). It also improves the frequency response of the amplifier. MOS transistor M3 is used in source-follower configuration for buffering and to drive external load. Since differential configuration is used, the other half of the circuit is replicated. The main reason for using differential configuration for the LNA is to avoid the use of balun, which is bulky and may degrade the performance of the LNA.

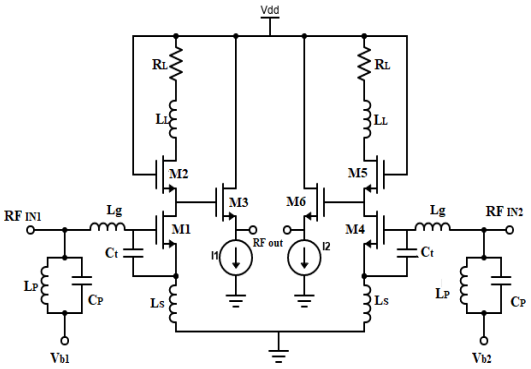

Figure 3. Proposed Ultra-Wideband LNA.

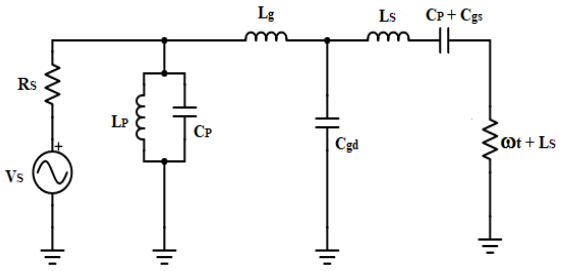

Figure 4. Section of LNA input network for impedance calculations.

4.1.1 Input-matching Analysis

Like in narrowband design, the reactive part of input impedance is resonated using two-section pass-band filter structure over the whole band from 3.1 to 8 GHz. Figure 4 depicts the section of LNA input network for input impedance calculations. As can be seen in Figure 4, the input impedance can easily be derived as given by Equation 3.

$$Z_{in}(s) = \frac{1}{s(C_{gs}+C_p)} + s(L_s+L_g) + \omega_T L_s$$
$$= \frac{s^2(L_s+L_g)(C_{gs}+C_p) + s\omega_T L_s(C_{gs}+C_p) + 1}{s(C_{gs}+C_p)} \quad (3)$$

where $\omega_T = \frac{g_m}{(C_{gs}+C_p)} = \frac{g_m}{C_t}$. The real part of Z_{in} is chosen to be equal to the source resistance; that is, $\omega_T L_s = R_s$. The gate-to-drain capacitance C_{gd} of MOS transistor M1 plays an important role in the resonance of the input circuit of the LNA. C_{gd} introduces one series resonance and one parallel resonance. The series resonance occurs between L_g and the parallel combination of L_s and C_{gd}. On the other hand, parallel resonance occurs between L_s and C_{gd}.

4.1.2 LNA Gain Analysis

To obtain the equation for the gain of the LNA, let us consider the transfer function of the filter section to be H(s). Hence, the input impedance is $\frac{R_s}{H(s)}$. Now, consider the current flowing into MOS transistor M1, which is, $v_{in}\left(\frac{R_s}{H(s)}\right)$. As we know, MOS transistor M1 acts as a current amplifier at high frequency with a current gain of $\beta(s) = \frac{g_m}{sC_t}$. Hence, the output current considering cascade stage is $\frac{v_{in}H(s)g_m}{(sC_tR_s)}$. Now, considering the load which is shunt peaking, the overall gain of the LNA can be obtained as given by Equation 4.

$$\frac{v_{out}}{v_{in}} = -\frac{g_m H(s)}{sC_t R_s} \frac{R_L\left(1+\frac{sL_L}{R_L}\right)}{1+sR_L C_{out}+s^2 L_L C_{out}} \quad (4)$$

where R_L is the load resistance, L_L is the load inductance and C_{out} is the total capacitance between the drain of MOS transistor M2 and ground.

4.1.3 LNA Noise Analysis

There are mainly two noise contributors in the proposed LNA. The first is the input network and the other is the noise of MOS transistor M1. Quality factor Q of the inductors in the input network decides the noise contribution from this network. The higher the quality factor Q for a given inductance value, the lower will be the noise. The noise cancellation techniques suggested in [8] can also be used for improving the noise performance of the LNA. Noise from MOS transistor M1 is due to drain current noise i_{nd} and gate-induced noise i_{ng}. Drain current noise is due to thermal agitation of carriers in the channel; while gate-induced noise is due to coupling of fluctuating channel charge into gate terminal. Noise due to both drain and gate is given by Equation 5 and Equation 6, respectively.

$$i_{nd} = 4kT\gamma g_{do} \quad (5)$$

$$i_{ng} = 4kT\delta \frac{\omega^2 C_{gs}^2}{5g_{do}} \quad (6)$$

where γ and δ are the noise parameters and g_{do} is the conductance for V_{DS}=0. There exists a correlation between drain current noise and gate noise. The correlation coefficient is represented by c and is $\approx j0.4$. By using classical noise optimization theory, the noise figure of the proposed UWB LNA can be derived as given by Equation 7.

$$F = 1 + \frac{P}{g_m R_s}\frac{\gamma}{\alpha} \quad (7)$$

where

$$P = \frac{p^2\alpha^2\chi^2(1-|c^2|)}{1+2|c|p\alpha\chi+p^2\alpha^2\chi^2} + \omega^2 C_t^2 R_s^2(1+2|c|p\alpha\chi+p^2\alpha^2\chi^2$$

where $P = {}^{C_{gs}}\!/_{C_t}$, $\chi = \sqrt{{}^{\delta}\!/_{(5\gamma)}}$, $\alpha = {}^{g_m}\!/_{g_{do}}$

Equation (5) gives the noise in the LNA due to MOS transistor M1, which is the main noise contributor. However, noise figure can be worse due to noise contributions from cascade MOS transistor M2 and output buffer MOS transistor M3. Considering noise and gain match along with the input match, the aspect ratio values of devices and values of input network components are given below in Table 1 and Table 2, respectively.

Table 1. Sizes of MOS devices.

No.	Device	Size
1.	MOS M1 and M4	280µm
2.	MOS M2 and M5	60µm
3.	MOS M3 and M6	100µm

Table 2. Values of components.

No.	Component	Values	No.	Component	Values
1.	Inductance Lp	2.5nH	5.	Capacitance C_t	100pF
2.	Capacitance Cp	340fF	6.	Load Inductance L_L	2.85nH
3.	Gate Inductance L_g	1.65nH	7.	Load Resistance R_L	110Ω
4.	Source Induct. L_s	720pH			

4.2 UWB Mixer Design

Down-conversion mixer is an important block in the UWB receiver. Like in the LNA, selecting a suitable down-conversion mixer for UWB range is a challenging task. Linearity of the UWB mixer decides the dynamic range of the receiver front end [9]-[10]. The linearity of the receiver is dominated by the mixer circuit. Many techniques have been suggested in literature for improving the linearity (IIP3) of the mixer. In [11], the third-order intermodulation (IM3) cancellation technique has been suggested for improving the IIP3 of mixer. Hence, UWB mixer should have good linearity, low noise and minimum power consumption. Various architectures for down-conversion mixers have been studied. Folded Gilbert mixer proposed in this paper satisfies the linearity, conversion gain and noise figure. It also consumes much less power due to its folded architecture.

Figure 5 depicts the schematic diagram of the proposed UWB down-conversion folded Gilbert mixer used in the receiver front end. The differential pair of NMOS transistors M1 and M2 forms the trans-conductance stage. PMOS transistors M3 through M6 are used in the LO stage, which is folded with respect to the trans-conductance stage. The output AC current from the trans-conductance stage should flow into the LO switches of PMOS transistors M3-M6. This can be achieved by using inductors L1 and L2 to provide high impedance. The folded architecture is preferred, as it significantly reduces power dissipation. NMOS Mb1 and Mb2 are used to provide biasing to the trans-conductance stage. The aspect ratio values of devices and values of components are provided in Table 3 and Table 4, respectively.

Table 3. Sizes of MOS transistors.

Sr. No.	Device	Size
1.	NMOS M1 and M2	50µm
2.	PMOS M3 – M6	100µm
3.	NMOS M0	240µm

Table 4. Values of components.

Sr. No.	Components	Values
1.	Inductors L1 and L2	5.5nH
2.	Bias Resistors R_b	440Ω

4.3 Band Pass Filter Design

An IF band pass filter has been designed to minimize the linearity requirements on the whole receiver chain and to eliminate the need for an external IF filter. Although on-chip BPF is not essential, it has been designed, as there may be multiple UWB transceivers operating in its vicinity, which may cause the problem of channel selection. There were two alternatives for filter selection; one is the active filter and the other is the passive filter. Active filters have traditional advantages of less area and excellent tuning over a wide range. But, they suffer from the main drawback of poor noise performance due to active components like MOS transistors. The noise performance is critical particularly at high frequency and wide bandwidth. The main objective of this research is to optimize the performance over cost (area). The passive filter has been selected. A traditional third-order Chebyshev band pass filter as depicted in Figure 6 has been designed.

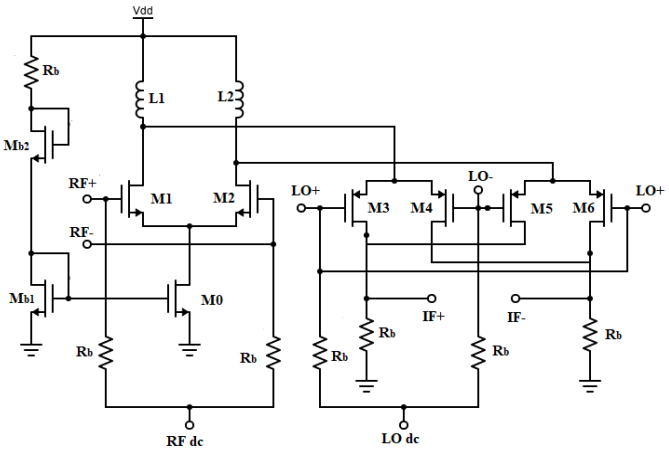

Figure 5. Proposed UWB folded Gilbert mixer.

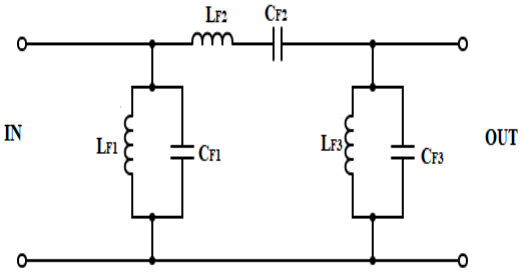

Figure 6. A typical LC band pass filter.

The filter with an IF center frequency of 2.64 GHz and a bandwidth of 528MHz was designed. This band pass filter improves the gain compression and intermodulation distortion of the IF downconverter. Table 5 gives the component values of the band pass filter.

Table 5. Values of components.

Sr. No	Components	Values
1.	L_{F1} and L_{F3}	520pH
2.	L_{F2}	2.5nH
3.	C_{F1} and C_{F3}	340fF
4.	C_{F2}	720pF

Jordanian Journal of Computers and Information Technology (JJCIT), Vol. 08, No. 02, June 2022.

5. RESULTS AND DISCUSSION

The UWB receiver which consists of an LNA, a mixer and an IF band pass filter, is designed and simulated in 1P6M UMC 180nm CMOS technology. The complete schematic of the proposed UWB receiver is shown in Figure 7 and its layout in 1P6M UMC 180nm CMOS process is shown in Figure 8. The receiver occupies an active area of 2.55mm^2. As the proposed design contains a large number of on-chip inductors instead of active inductors, all of its performance parameters are optimized instead of area, which was the main objective of this research. In this section, schematic and post-layout simulation results of the LNA and the mixer are presented and discussed first, followed by receiver results. The heterodyne receiver is formed by directly connecting the output of the LNA to the mixer stage without any inter-stage matching for maximum voltage gain.

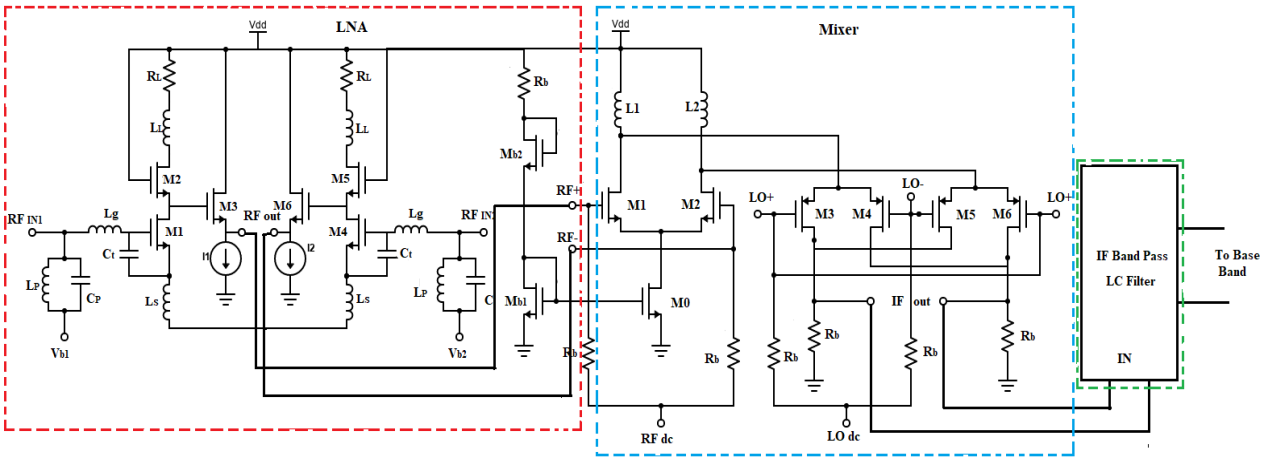

Figure 7. Complete schematic of the proposed UWB receiver front end.

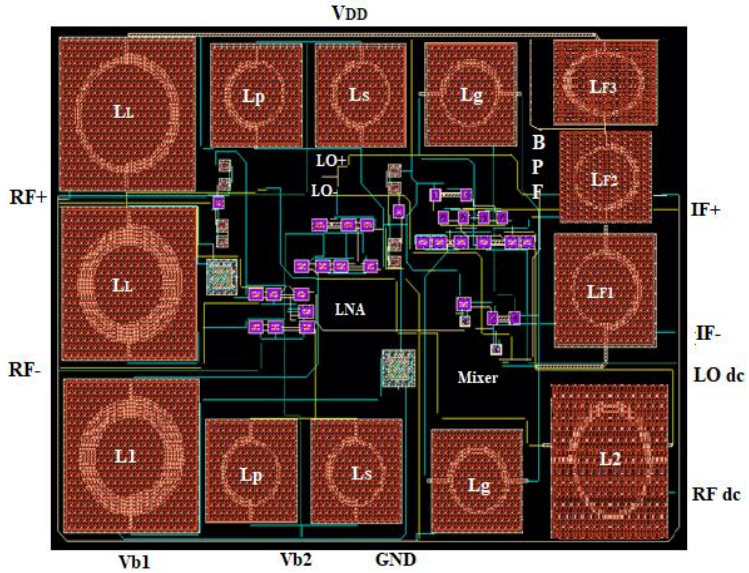

Figure 8. Layout of the proposed UWB receiver front-end.

5.1 LNA and Mixer Results

The post-layout simulated result of the UWB LNA gives excellent input matching (S11) of lower than -10dB over the entire range of 3.1 to 8GHz, whereas the gain (S21) of the LNA is from a minimum of 12.6dB to a maximum of 19.5dB, as shown in Figure 9. The fall of gain by 3dB is compared to schematic results. The fall in gain is due to parasitics generated while extracting the of layout. The LNA also shows a good noise figure of 5.1dB to 7.32dB over the entire range of interest, as shown in Figure 10. The noise figure also degrades by ±1dB due to parasitics of layout.

The schematic and post-layout simulation results depicted in Figure 11 show excellent reverse isolation (S12) of -66.8dB and -58.1dB, respectively, due to the cascode architecture used, which is

primarily used for improving isolation. The output matching (S22) as depicted in Figure 11 is also below -10dB in both schematic and post-layout simulation results. The LNA consumes 10.5mA at a supply voltage of 1.8V.

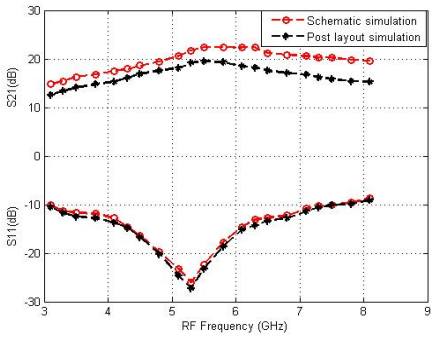

Figure 9. Simulated S11 and S21 of the LNA.

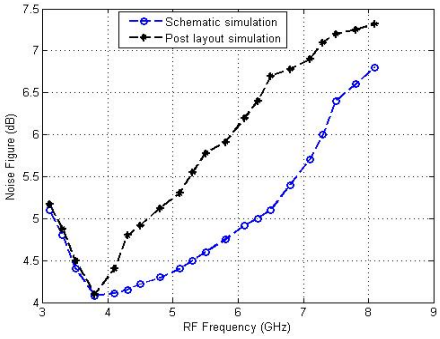

Figure 10. Simulated noise figure of the LNA.

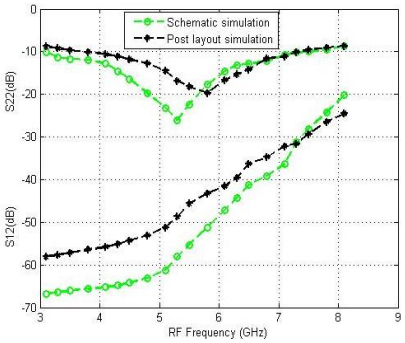

Figure 11. Simulated S12 and S22 of LNA.

Figure 12 shows the conversion gain (CG) and noise figure (NF) plot of the folded Gilbert mixer. The mixer has a schematic CG of 11.48dB to 14.68dB and a post-layout simulation CG of 10.78dB to

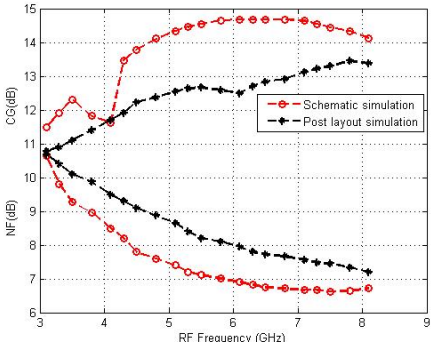

Figure 12. Simulated CG and NF of the mixer.

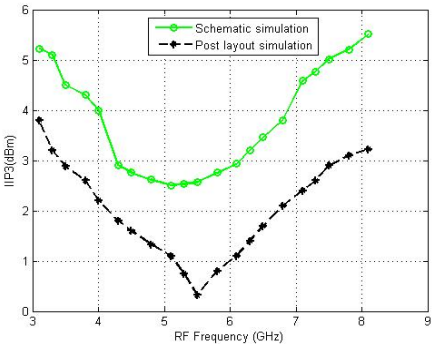

Figure 13. Simulated IIP3 of the mixer.

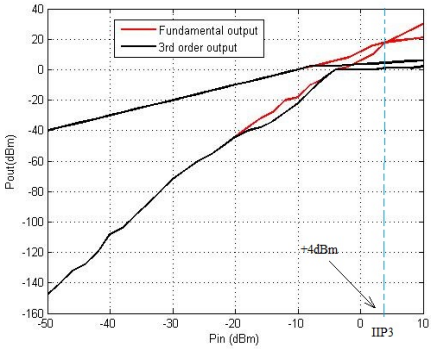

Figure 14. Simulation for IIP3 of the mixer at 4GHz.

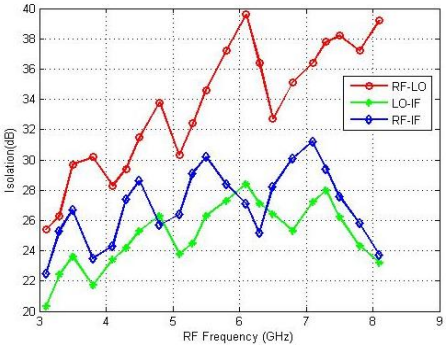

Figure 15. Mixer isolation *vs* RF frequency.

13.45dB over the entire band of 3.1 GHz to 8.1GHz. The mixer shows an NF of 6.8dB to 10.7dB for schematic simulation and an NF of 7.2dB to 10.6dB for post-layout simulation over the entire band of interest, which is acceptable when used with LNA in the receiver. Figure 13 depicts the IIP3 which is a measure of linearity of the mixer as a function of RF frequency. It shows excellent linearity of +2.5dBm to +5.5dBm in schematic simulation and slightly degraded linearity of +0.32 to +3.8dB in post-layout simulation. Figure 14 depicts the main signal power and third-order intermodulation power as function of the RF input power. The two-tone test is performed to calculate the IIP3 at a particular RF frequency. The two signals are fed to the RF input port, one at 4GHz and the other at 4.001GHz. The LO signal has a frequency of 3.9505GHz and a power level of -5dBm. The proposed folded Gilbert mixer exhibited an input third-order intercept point (IIP3) of +4dBm at an RF frequency of 4GHz. This result has been confirmed in Figure 13 as well. The port-to-port isolations of the proposed mixer were simulated and are presented in Figure 15. The port-to-port isolation represents the amount of leakage between the mixer ports. It is found that the mixer has an RF-LO isolation of better than 25dB, an LO-IF isolation of better than 20dB and an RF-IF isolation of better than 22dB. Due to folded architecture used in the mixer, it consumes only 7mA from a 1.8V supply.

5.2 Receiver Results

The UWB heterodyne receiver is implemented with the LNA, mixer and IF band pass filter as discussed in Section 2 with external LO signal. Due to differential architecture of the LNA, its output is directly connected to the mixer. The schematic simulation and post-layout simulation results of the complete receiver are presented. The receiver when simulated shows that the gain varies from 18.2dB in Band 1 (3.1GHz) to 22.8dB in Band 5 (5.5GHz) and is 19.6dB in Band 8 (7.1GHz), as shown in Figure 16. Similarly, the post-layout simulation results show that the gain varies from 15.4dB in Band 1 (3.1GHz) to 19.8dB in Band 5 (5.5GHz) and is 18.1dB in Band 8 (7.1GHz). The drop in the gain in the post-layout simulation is less than 1% to 2% and is well within the targeted specifications. This variation in the gain is not significant due to the variation of received signal strength over the frequency range [19]. It is found that the receiver gain drops by approximately 2dB at each band edge. But this drop in the gain has a negligible effect because the ten carriers at the band edge are guard carriers [1]. The receiver input matching (S11) is depicted in Figure 16 for schematic simulation and post-layout simulation. For schematic simulation, it is better than -10dB, whereas for post-layout simulation, S11 is better than -9.2dB over the entire range of 3.1GHz to 8.1GHz, as shown in Figure 16. Figure 17 depicts the IIP3 *versus* RF frequency of the receiver for both schematic and posts-layout simulations results. The IIP3 varies between -5.1dBm and -2.2dBm for schematic simulation and varies between -6.3dBm and -2.9dBm for post-layout simulation. This IIP3 is excellent for the UWB receiver to overcome cross-modulation distortions. The NF varies between 4.1dB and 7.1dB for schematic simulation as depicted in Figure 18. Figure 18 also depicts the post-layout simulation result for NF, which varies between 4.8dB and 8.92dB. The degradation in NF is due to parasitics in the post-layout extracted. This variation, which is acceptable, is due to variation of gain of the LNA. The receiver also has an excellent reverse isolation (S12) of -42dB to -59dB for schematic simulation and -32.1db to -54.2dB for post-layout simulation. The UWB receiver consumes 17.5mA at a supply voltage of 1.8V.

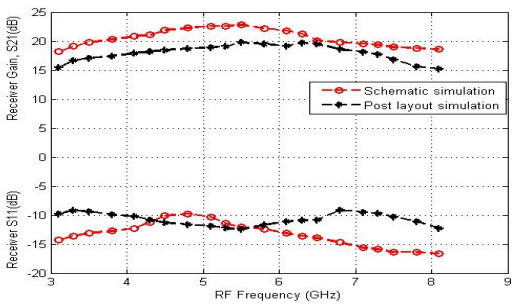

Figure 16. Receiver gain and S11.

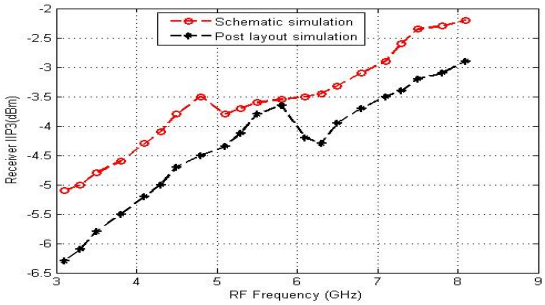

Figure 17. Receiver IIP3 *versus* RF frequency.

Table 6 summarizes the post layout simulated performance parameters of the proposed UWB heterodyne CMOS receiver front end and comparisons with recently published similar work are also listed. It can be seen that the proposed receiver has optimized performance parameters. The comparative study further reveals that although the area of 2.55mm^2 is comparatively large due to full

integration including all inductors, the performance parameters can still be optimized. Further work can be carried out in deep-submicron technology node like 65nm or better to further reduce the active die area. The transmitter for the UWB [20] can also be implemented in future work so that a complete transceiver can be fully integrated for UWB applications.

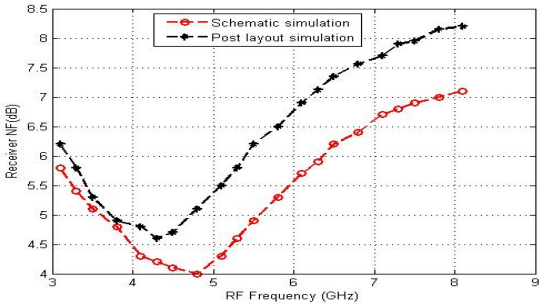

Figure 18. Receiver NF *versus* RF frequency.

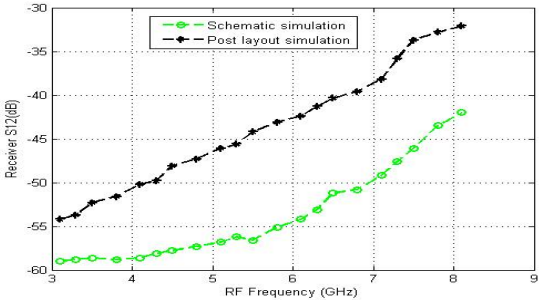

Figure 19. Receiver S12 *versus* RF frequency.

Table 6. Performance comparison with recent works.

	This Work	[12]	[13]	[14]	[15]	[16]	[17]	[18]
Tech.	180nm	180nm	180nm	180nm	180nm	180nm	180nm	180nm
BW (GHz)	3.1 - 8.1	3 - 11	7.1 – 8.1	3.1 –10.6	3.1–10.6	1-6	4-10	3.1-10.6
Gain (dB)	15.2-19.8	22.8-25.8	22- 42	29	19.5-23.3	23-25	18-32	73.5
NF (dB)	4.8-8.9	4.9- 6.9	4.7	4-5.1	5.2- 9.1	2.2-2.8	3-6	8.4
IIP3 (dBm)	-6.3 to -2.9	-26	NA	-14	-10.4	-5.2 to -3.5	-6	NA
Area (mm^2)	2.55	1.04	1.43	NA	NA	3.24	2.88	3.3
Pdc (mW)	31.5	39.2	65	31.5	42	18	23	88.74

6. CONCLUSION

A 3.1GHZ – 8.1GHz CMOS UWB heterodyne receiver front end is proposed, simulated and analyzed in this paper. The proposed receiver architecture consists of a UWB LNA, a down-conversion UWB folded Gilbert mixer and an IF band pass filter. Designed and simulated in 1P6M UMC 180nm CMOS technology, the proposed receiver has optimized performance parameters as: NF of 4.8-8.9dB, gain (S21) of 15.2-19.8dB, IIP3 of -6.3dBm to -2.9dBm, consuming 17.5mA from a 1.8V supply and occupying an area of 2.55mm^2. Future research is required to design and fully integrate UWB trans-receiver for various applications.

ACKNOWLEDGEMENTS

The authors would like to thank the Ministry of Electronics and Information Technology (MeitY), Government of India for the EDA tool funding and support.

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ملخص البحث:

تقترح الورقة نهايةً أماميةً مبتكرةً ومؤمثلةً بالكامل لمستقبل تردّدات راديوية فائق عرض النّطاق التّردّدي باستخدام تقنية سي موس (UMC 180nm IP6M CMOS). والجدير بالذكر أن المعمارية الهتردودينية المستخدمة في هذا العمل لا تستخدم مازج نَبْذ الخيال المجمَّع على الدارة المتكاملة. ويتألف المستقبِل المقترح من مكبّر تفاضلي منخفض الضّجيج ذي مراحل متعاقبة موصولة بنمط المنبع المشترك (CS) ومترابطة حثّياً، ومازج تحويل الى أسفل مطوي من جوع جلبرت. ويعمل المكبّر التفاضلي منخفض الضّجيج على إلغاء استخدام بالون فعّال محسِّناً الأداء المتعلّق بالضّجيج، بينما تعمل المعمارية المطوية على تقليل استهلاك الطّاقة بالنسبة للمكبّر. وقد بينت نتائج المحاكاة بعد التّصميم أنّ المكبّر لَهُ كسْب فولتية مقداره من (15.2) و(19.8) ديسيبل، ورقم ضجيج بين (4.8) و(8.9) ديسيبل، ونقطة تقاطع مدخل (IIP3) بين (6.3-) و(2.9-) dBm. كما يستهلك المكبّر ما مقداره (31.5) ميلي واط من مصدرٍ ذي فولتية قدرها (1.8) فولت. كذلك يمتلك المكبّر عَزْلاً عكسياً جيداً (S12) بين (42-) و (59-) ديسيبل بسبب التركيب التعاقبي، ويحتل مساحة قدرها 2.55 ملم^2.